MODELING AND CONTROL OF MODULAR MULTILEVEL DC-DC SWITCHED-CAPACITOR POWER CONVERTER

A Dissertation
Presented to
The Academic Faculty

By

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology

December 2018

MODELING AND CONTROL OF MODULAR MULTILEVEL DC-DC SWITCHED-CAPACITOR POWER CONVERTER

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To My Beloved Wife Hui Ding and Our Dear Parents.

ACKNOWLEDGEMENTS

First of all, I would like to express my sincere gratitude to my advisor, Professor Maryam Saeedifard, for her continuous support to me throughout my PhD life. I could not have achieved my study goals and gained such a great PhD experience without her professional guidance, insightful advice and financial support. In addition, I am truly grateful to the space she gave me to explore, experiment and improve my own ideas and the access to various related projects for a more comprehensive background. I also greatly appreciate her patience and encouragement when I face challenges and difficulties along the way. It has certainly been a very exciting and rewarding journey thanks to all the help from her.

Furthermore, I would like to thank Professors Lukas Graber, Sakis Meliopoulos, Santiago Grijalva and Oleg Wasynczuk for serving in my examination committee and for their insightful feedback and advice to my PhD thesis. Especially, I would like to thank Professor Graber for involving me in a very interesting and cutting-edge cryogenic power converter project, and Professor Wasynczuk for his valuable advice and encouragement during projects at the very beginning of my PhD journey. Special thanks also go to Professor Ronald Harley for his help, support, encouragement and valuable advice during the Haiti solar charger project.

I would also like to thank the many great fellow students and friends I met during my PhD. Special thanks go to Professor Jiangchao Qin, Dr. Heng Yang, Dr. Hao Chen, Dr. Nan Liu, Dr. Yi Deng, Dr. Chen Jiang and Dr. Liangyi Sun, for many inspiring discussions and advice on both my study and professional development. I also would like to thank my friends Dr. Minyu Cai, Jinyuan Tian, Hang Shao, Jingfan Sun, Qichen Yang, Xiangyu Han, Chanyeop Park, Sufei Li, Shen Zhang, Cheng Gong, Liran Zheng, Chunmeng Xu, Jia Wei and many more for their friendship and help during the course of my doctoral studies.

Finally, I would like to thank my wife and our parents, for their unconditioned love and constant support.

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SUMMARY

The Modular Multilevel Clamped Capacitor Converter (MMC3) is an attractive switched-capacitor DC-DC converter topology for applications with high output/input voltage conversion ratio (CR), featuring reduced voltage stress of power devices, high power density, bi-directional power flow capability and a modular structure. In most DC-DC converter applications, feedback output voltage control, which allows the converter to output and maintain a preset level of voltage during both normal operation and source/load transients, is desired. However, the voltage CR of the conventional MMC3 is fixed by the number of series-connected identical submodules (SMs), and an effective feedback control of output voltage is not yet available. In addition, large-amplitude current spikes may occur in the MMC3 due to the parallel connection of SM capacitors with imbalanced voltages, which lead to additional power losses and reliability issues. The impacts of parasitic inductances in the power loop also need to be thoroughly analyzed. Furthermore, to expand the achievable output voltage range of the MMC3 and enhance its reliability based on its modular structure, a procedure to reliably bypass/insert SMs during operation is also required, such that the number of SMs can be varied.

The purpose of this research is to address the aforementioned technical challenges associated with the design, operation and control of the MMC3. A detailed time-domain model along with a small-signal state-space model have been derived for the MMC3. A closed-loop voltage control strategy for the MMC3 has been proposed based on the developed models, which regulates its output voltage by utilizing the impact of the Pulse Dropping Technique (PDT) and insertion/bypass of SMs. The developed models and proposed control strategy are validated by both simulation studies in MATLAB and LTSPICE environments as well as experimental studies on a compact 170-W Dickson converter prototype designed and built with GaN FETs, which achieves 93.8% efficiency. A brief summary of future work is provided in Chapter 8.

CHAPTER 1
INTRODUCTION

1.1 Background

DC-DC converters with high voltage conversion ratio (CR) are attractive converters for a number of applications such as data center power distribution system [1], photovoltaic energy conversion [2] and hybrid electric vehicle (HEV) power management system [3]. The conventional buck/boost converters have significant drawbacks for these applications due to extreme duty ratios and the usage of overrated components, leading to increased power losses and reduced power density. On the contrary, Switched-Capacitor (SC) power converters offer improved power density and system efficiency with high CR by eliminating the use of bulky inductors and using semiconductor devices with reduced ratings [4]. Among various SC converter topologies, the Modular Multilevel Clamped Capacitor Converter (MMC3) stands out with several desirable features, including reduced voltage stress of power devices, high power density, bi-directional power flow capability and a modular structure [5, 6].

Recently, the Wide Band-Gap (WBG) switching devices, particularly GaN devices, have become attractive switching devices for power electronic systems due to their unique electrical and thermal capabilities/characteristics compared to their Si counterparts, enabling considerable reduction of device losses and thermal management effort and increased switching frequency and power density [7, 8, 9, 10, 11]. However, the commercially available GaN power devices are only rated up to 650 V. With reduced component voltage stress of the MMC3, GaN devices are potential candidates to be used for the MMC3 to further improve system efficiency and power density at high switching frequencies.

1.2 Problem Statement

Despite the aforementioned features of the MMC3, its application in power electronic systems, due to several technical challenges, has been limited [2]. Traditionally, the output voltage of the MMC3 can be only fixed integer multiples/aliquots of the input voltage, and the existing open-loop MMC3 can neither output a preset level of voltage nor stabilize the output voltage when subjected to any transients/disturbances, either in the source or output load [12]. Thus, an effective closed-loop output voltage control that maintains the key advantages of the MMC3 is desired. In addition, large-amplitude current spikes occur between paralleled SM capacitors with imbalanced voltages in the conventional MMC3, which causes additional power losses and reliability issues. Thus, inductive components need to be carefully designed and inserted between SMs to reduce the current spikes and enable resonant operation of the MMC3 under various operating scenarios. On the other hand, the capability to insert/bypass SMs of the MMC3 is needed to expand the range of its achievable output voltage, and to bypass/replace any faulty SMs with redundant SMs to maintain the normal operation of the converter. However, a procedure to reliably insert/bypass SMs of the MMC3 with inductive components and under various control schemes is needed to avoid current spikes and integrate with the proposed control method.

1.3 Objective of the Proposed Research

The objective of the proposed research is to address the technical issues associated with the design and control of the MMC3. The proposed research is summarized as follows:

1. Derive detailed time-domain and state-space models for the MMC3;

2. Propose an effective feedback control strategy for the MMC3 based on derived models;

3. Improve the efficiency and power density of the MMC3 by using GaN power devices;

4. Integrate a reliable SM bypass/insert function into the proposed control.

5. Design and implement a hardware prototype based on a multi-objective optimal design procedure to validate the proposed control strategy and discuss the tradeoffs.

CHAPTER 2
LITERATURE SURVEY

2.1 Overview of Wide Bandgap (WBG) Power Devices

In recent years, the WBG power devices, especially SiC and GaN power devices, have attracted significant research efforts due to their superior physical characteristics such as high thermal conductivity and electrical characteristics including low on-state resistance, input and output charges and fast-switching capability, which all lead to promising improvements in efficiency and power density. In this section, an overview of SiC and GaN power devices along with their integration challenges are provided.

2.1.1 SiC Power Devices

Among SiC switching devices, SiC Schottky diodes with voltage and current ratings of up to 1200 V and 50 A, respectively, have been recognized for their near zero reverse recovery current/time and, subsequently, significantly low power losses in hard switching applications [13]. SiC Schottky diodes have been broadly used in power electronic circuits with hybrid combination of Si and SiC semiconductor devices, particularly as the anti-parallel diodes of the controllable Si switched in bi-directional switch configurations. For controllable SiC switches, there are three types of SiC switches available: SiC JFETs, SiC BJTs and SiC MOSFETs [14].

SiC JFETs with voltage and current ratings of 1200 V and 50 A, respectively, have been reported to have a significantly low on-state resistance and very high switching speed due to their small intrinsic capacitances. SiC JFET is able to conduct current in both directions, which can be potentially used for bi-directional switches without any requirement for anti-parallel diodes [15], [14]. However, the normally-off SiC JFET seems to disappear from the

market and all of currently available SiC JFETs are normally-on devices, which suffer from the requirement to an additional low-voltage MOSFET in series, i.e., cascode arrangement [14]. SiC BJT is a current-driven device and, consequently, need a continuous base current while conducting. For high-voltage applications such as the MMC, the power consumption of the gate driver will add to the MMC power losses. The gate driver loss of the SiC BJT is almost independent of the switching frequency while for SiC JFET, it is proportional to the switching frequency [16]. Besides, SiC BJT has a higher on-state resistance than the SiC JFET, which leads to higher conduction losses.

SiC MOSFET is a normally-off device with a simple gate driver requirement. The emergence of SiC MOSFET enables direct substitution of Si MOSFETs for many applications. In the technical literature, performance of SiC MOSFET with a traditional Si MOSFET and a Si IGBT for various applications have been evaluated and improvement of SiC MOSFET over the Si counterparts in terms of lower power losses, higher switching speed, and lower temperature rise under the same output power, has been reported [17, 18, 19, 20].

2.1.2 GaN Power Devices

Although GaN devices have great electrical characteristics such as very low on-resistance and super fast switching speed, one basic problem is that GaN devices are essentially normally-on devices, which is not desirable in most power electronic systems. In order to make the GaN devices normally off while maintaining their advantages, extensive research and development efforts have been put into GaN power devices. There are mainly three types of normally-off GaN power devices available currently, namely the GaN FET [7], the cascode GaN HEMT [21] and the GaN Gate Injection Transistor (GIT) [22].

The GaN FET is a widely used device due to its normally-off operation, superior electrical performance and availability in different voltage and current ratings [7]. However, the narrow range of acceptable gate voltage has brought challenges for gate drive circuit design. For EPC GaN FETs, the devices normally have a turn-on threshold voltage of less

than 2 V, a norminal turn-on gate voltage of 5 V, a maximum positive voltage of 6 V and a maximum negative voltage of -1 V. The narrow range of operating gate voltages make GaN FETs vulnerable to shoot-through or gate damage issues caused by cross-talk and noise [23]. On the other hand, the normally-on GaN device can be combined with a Si MOSFET in a cascode structure and function like a normally-off device [21]. By using this method, commercially available gate drivers for Si MOSFET can be used, and superior characteristics of GaN device can be utilized. However, the use of Si MOSFET causes delays in driving the GaN device, thus slowing down its switching speed. The existence of Si MOSFET also make it more difficult to model the device and design for soft-switching [24]. The GIT has achieved very high efficiency in power electronic systems. However, the use of it is mainly limited in terms of availability.

The commercially available GaN power devices are rated up to 650 V [7]. Thus, while SiC devices rated more than 1200 V are suitable for applications that previously use Si IGBTs, the GaN power devices currently are more suitable for lower-voltage applications, which used to rely more on Si MOSFETs.

2.1.3 Issues of using WBG Power Devices

Cross-talk

When Wide Bandgap (WBG) power devices are used, special attention needs to be paid to the reliability issues related to driving them. Due to the faster switching speed and smaller range of tolerable gate voltage, even when sufficient dead-time has been applied, the WBG devices are vulnerable to the cross-talk issue [23]. The cross-talk issue arises from the parasitic capacitances of the power MOSFET as shown in the the equivalent MOSFET model in Fig. 2.1. There are three parasitic capacitances associated with the power MOSFET. C_{ds}, which is also called the output capacitance, mainly used to analyze the rise and fall of the drain-source voltage. C_{gs} is the gate capacitance of the device. When the voltage of the C_{gs} reaches the threshold of the device, its channel is turned on, and vice versa. C_{gd} is also

called the Miller capacitance. During the turn-on and turn-off transients, when the drain-source voltage is changing rapidly, majority portion of the gate current will be through the Miller capacitance, leading to an almost constant "Miller plateau" level in the gate-source voltage. In many device datasheets, another set of parasitic capacitances may be given in the name of input capacitance C_{ISS}, reverse transfer capacitance C_{RSS} and output capacitance C_{OSS}. The values of parasitic capacitance defined in Fig. 2.1 can be calculated by these values through equation (2.1). Besides the three parasitic capacitances, other modeling components include an ideal switch S and the on-state resistance $R_{ds,on}$, which are used to model the channel of MOSFET, and a body diode. Based on this equivalent model of the MOSFET, key waveforms during the turn-on and turn-off of the MOSFET can be derived [25].

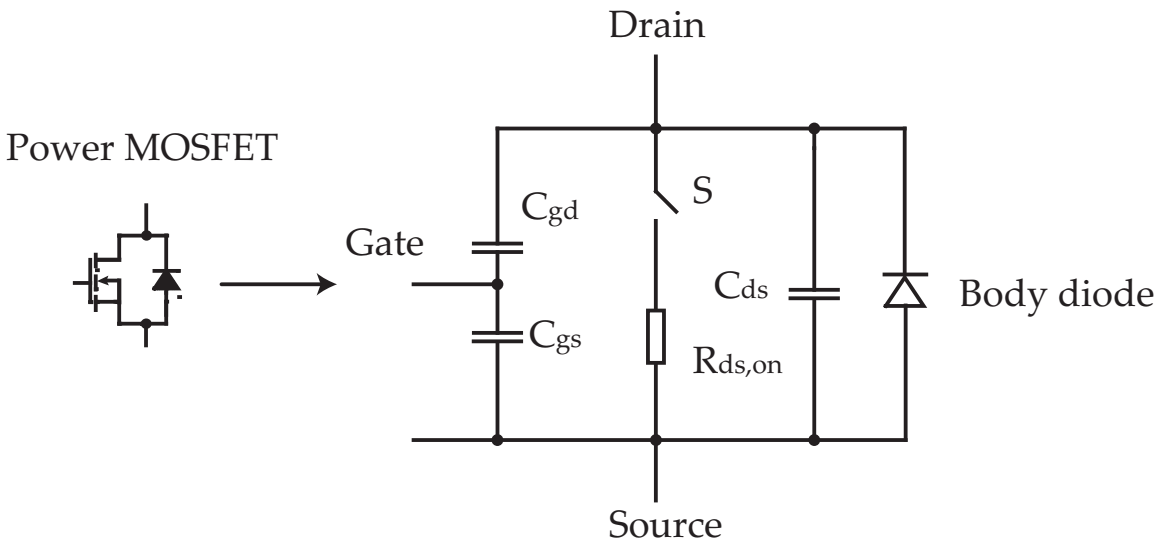


Figure 2.1: Model of the power MOSFET considering parasitic capacitances.

$$\begin{cases} C_{gd} = C_{RSS} \\ C_{ds} = C_{OSS} - C_{RSS} \\ C_{gs} = C_{ISS} - C_{RSS} \end{cases} \tag{2.1}$$

To illustrate the mechanisms of crosstalk, a basic half-bridge structure with inductive load is analyzed, which consists of two power MOSFETs driven complementarily [23]. The turn-on transient of the upper MOSFET is demonstrated in Fig. 2.2. Due to the dead-time, when the upper MOSFET turns on, the lower switch is already off, and its drain-source voltage will start to increase as its C_{ds} gets charged by the charging current flowing through the upper channel. However, as the lower switch is off, there exists another path for the charging current to flow, namely through the gate capacitances and the gate driver circuit. This will lead to a positive voltage showing up between the gate and source of the lower switch. If this positive voltage is close to the turn-on threshold of the MOSFET, it will temporarily turn-on the lower switch at the turn-on transient of the upper switch, leading to a shoot-through and even device failure [23]. On the other hand, during the turn-off transient of upper switch as shown in Fig. 2.3, the lower switch remains off during the transient. The drain current of the upper switch will start to drop while the inductive load current free-wheels through the body diode of the lower MOSFET and leads to a discharging current flowing through its capacitances. This current will also flow through the gate driver circuit, causing a negative voltage between the gate and source of the lower switch, adding to any applied negative gate voltage. This negative voltage may potentially over-stress the gate of the lower switch, especially for WBG devices, which cannot tolerate much negative gate voltage [23].

Reverse Conduction Mode

Unlike Si MOSFETs, special attention should be paid when using the body diodes or reverse-conduction capability of WBG devices to conduct reverse current in power electronic circuits according to related research [26, 27, 28]. For example, GaN FET does not have a body diode, but could conduct current in the reverse direction. However, the voltage drop during this phase is strongly dependent of the gate voltage supplied, and the power loss is higher compared with adding an external Schottky diode [27]. Thus, it is not rec-

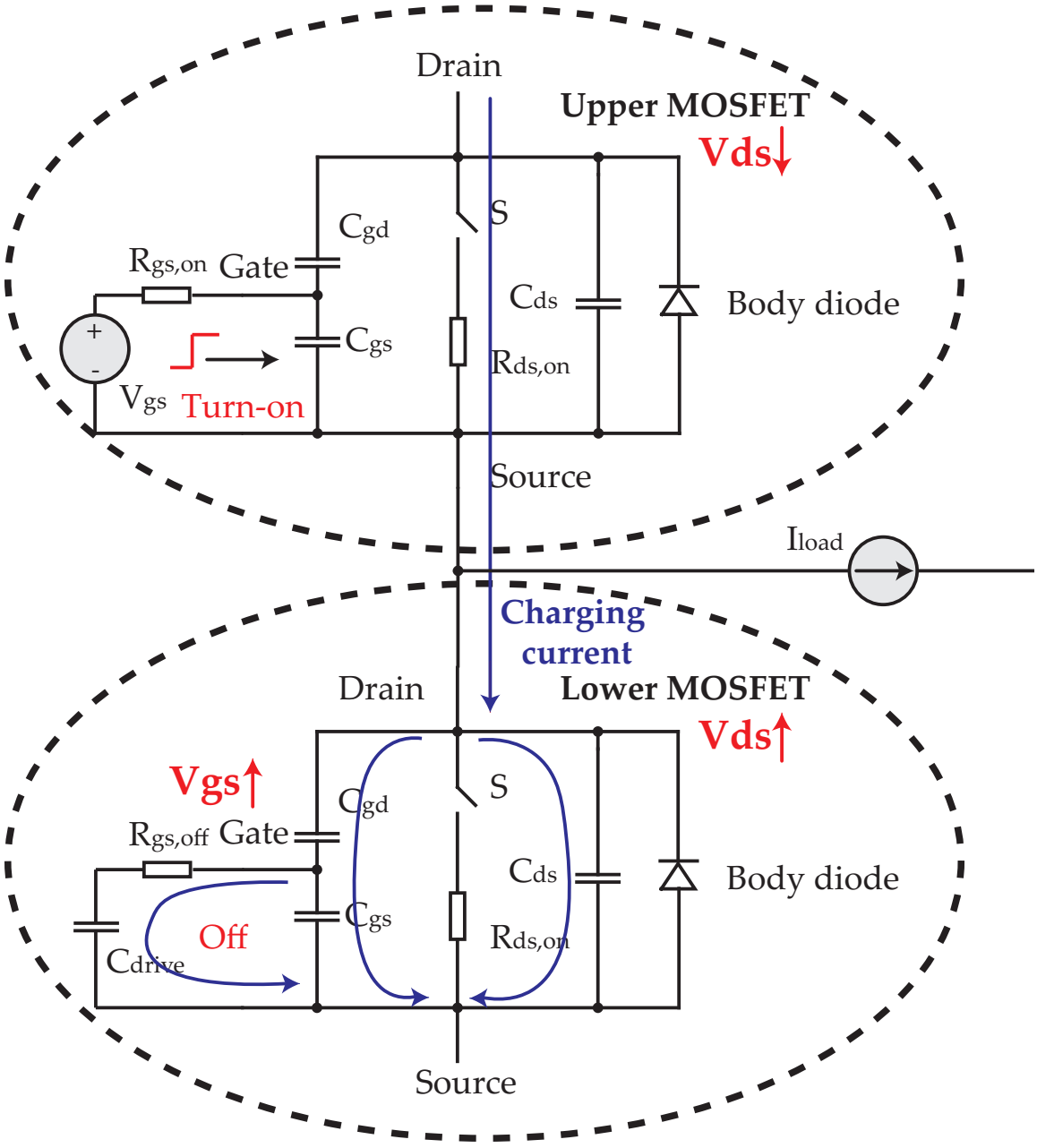


Figure 2.2: Cross-talk during the turn-on transient of the upper switch.

ommended to utilize the reverse conduction mode of GaN FET and an external diode is desirable to avoid excessive power loss that may even damage the power device.

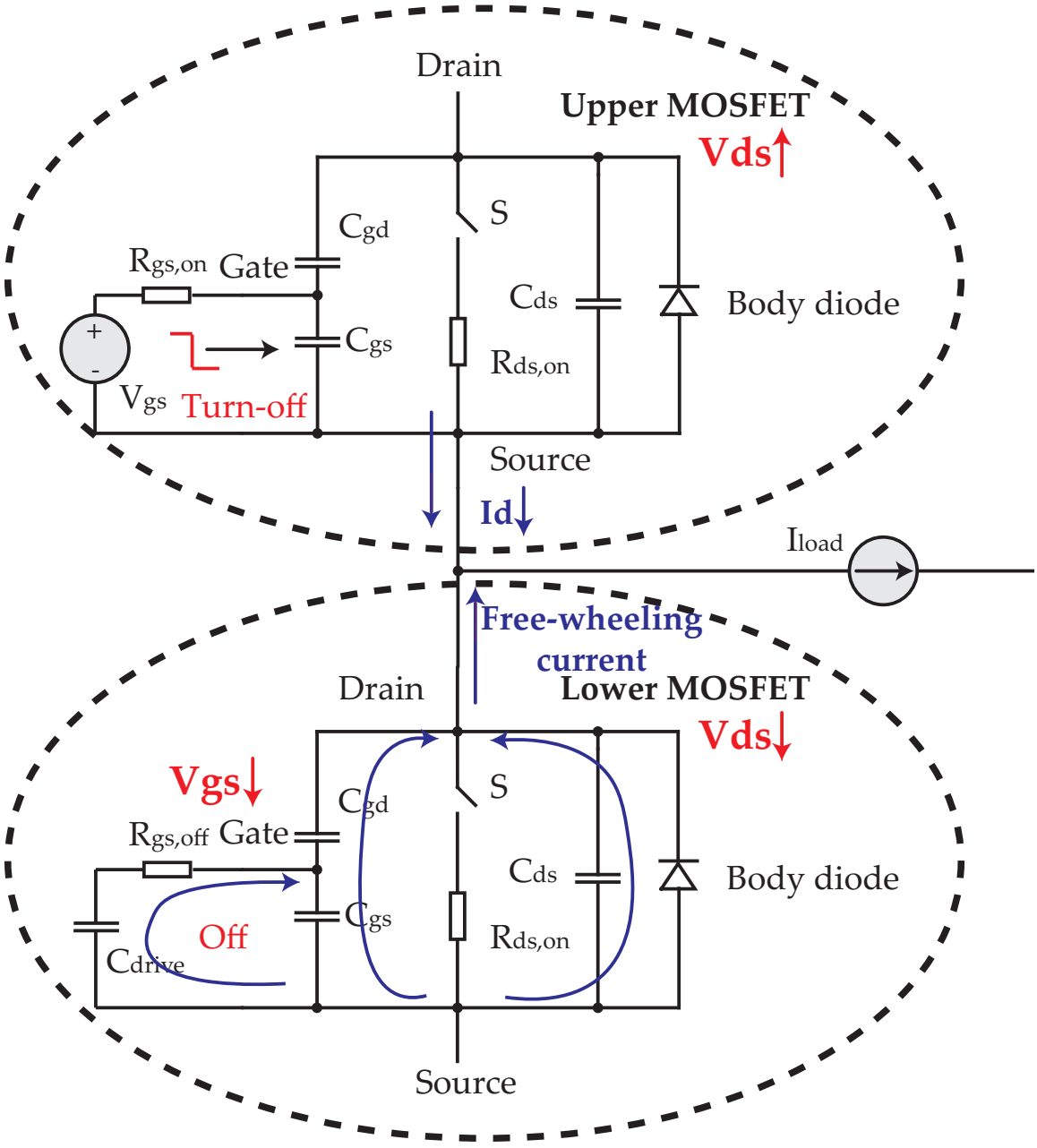


Figure 2.3: Cross-talk during the turn-off transient of the upper switch.

2.2 Electro-thermal Model of Power Devices

The WBG switching devices, particularly GaN devices, have become attractive switching devices for power electronic systems due to their unique electrical and thermal capabilities/characteristics compared to their Si counterparts, enabling considerable reduction of the size of passive components and thermal management effort and improvement of the ef-

ficiency and power density [7, 8, 9, 11, 29]. However, as the devices and power electronic systems become smaller, the heat dissipation becomes more difficult and new challenges are imposed on thermal management [10]. Therefore, at the design stage of GaN-based power electronic systems, it is necessary to determine the junction temperature profile of the switching devices to ensure that they operate within their safe operation area. The junction temperature also has significant impacts on the electrical performance of GaN FET devices, and therefore, for accurate temperature estimation, the device model needs to take the thermal impacts into account [30, 31]. Consequently, electro-thermal modeling of GaN devices is one of the important steps for system design/integration.

Despite the importance of electro-thermal modeling of GaN devices, as mentioned in [32], an electro-thermal model for the GaN FET that considers the device self-heating is not yet readily available. Efforts have been made to develop electro-thermal models for GaN HEMTs, which considered nonlinear thermal effects, self-heating effects and bias dependence [30, 33, 34], for radio frequency applications. Reference [31] presents electro-thermal models for both GaN vertical MOSFETs and GaN lateral HEMTs based on device physics. However, physical models generally involve many device parameters with mutual couplings, which make their implementation difficult for circuit simulation [35]. On the other hand, the results obtained from physics-based models may not be as accurate as those from behavioral models [36]. Thus, simple and accurate behavioral models are considered more favorable for circuit simulations. In addition, the existing electro-thermal models focus on the effect of junction temperature on the I_{ds}-V_{ds} relationship during the device conduction period. The thermal effects on the device switching characteristics, however, are only explored in terms of switching losses instead of parameters such as $\frac{dv}{dt}$ and $\frac{di}{dt}$, which are important for power loss evaluation, system reliability and EMI issues [30, 31, 32, 33, 34]. The PLECS toolbox is capable of providing a look-up table-based electro-thermal model for a power device at various temperatures and estimating the device temperature based on its power losses. However, the PLECS toolbox does not take the junction

temperature of a device as an input to include the temperature impact on the device characteristics [37]. Furthermore, the model in the PLECS toolbox focuses mainly on the power loss perspective and does not provide detailed transient waveforms as those obtained from circuit simulations. After all, no behavioral electro-thermal model for circuit simulation that considers both device static and switching characteristics has been developed for GaN FETs.

2.3 Overview of Switched-capacitor (SC) DC-DC Converter Topologies

Conventional switch-mode power converters rely on inductors and/or transformers to enable voltage conversion. These bulky inductive components add to the system volume and lead to decreased power density. In addition, the efficiency of the conventional power converters when the voltage conversion ratio (CR) is high drops due to overrated power devices and extreme duty ratios. On the other hand, SC DC-DC converters achieve voltage conversion using capacitors and eliminate the use of bulky inductive components. SC converters also enable the use of lower-rated power devices with reduced component stress [2, 4]. Thus, SC converters are attractive for applications where a high voltage conversion ratio is required and high power density is desired, e.g., data center power distribution system [1], photo-voltaic energy conversion [2] and hybrid electric vehicle power management system [3]. Among various SC DC-DC converter topologies, the flying-capacitor multilevel converter, the Dickson converter, and the MMC3 are the most extensively researched.

2.3.1 Flying Capacitor Multilevel DC-DC Converter (FCMDC)

The FCMDC is a multilevel SC converter topology that is shown in Fig. 2.4(a) and was first proposed in 2003 [38]. It has several advantages, including low device and capacitor count as well as reduced voltage stress of its devices [39]. However, the FCMDC has several disadvantages for high voltage-gain applications [39]. For an n-level FCMDC, there

exists n switching states and, thus, the complexity of control increases with the voltage-gain ratio. During each state, n devices are conducting current in series and the turn-off currents of the devices are n times of the load current [39], which induces relatively high conduction and switching losses. In addition, the asymmetric charging and discharging loops of the FCMDC make it difficult to realize Zero-Current Switching (ZCS) by utilizing stray inductances [39]. Thus, the practical voltage-gain ratio of the FCMDC is limited to 2 or 3 [39].

A hybrid FCMDC converter, known as the Flying Capacitor Multilevel (FCML) converter as shown in Fig. 2.4(b), has also attracted significant attention [40, 41, 42, 43]. The FCML can be viewed as a combination of the conventional FCMDC and an inductive component that makes soft switching and resonant operation possible, thereby improving the efficiency [42]. However, the problems of increasing switching states, conducting devices and switching current still remain a challenge for the FCML as well.

2.3.2 Dickson Converter

The Dickson converter, also known as the Charge Pump, was first proposed in 1976 due to the need of on-chip high-voltage generation [44]. The topology of an $(n+1)$-level Dickson converter is shown in Fig. 2.5. The Dickson converter is intensively studied due to its advantages including efficient utilization of power transistors with reduced voltage ratings for high voltage-gain applications and simplicity of control with only two operating states [4]. However, due to the use of diodes, the Dickson converter is not modular and can only allow unidirectional power flow.

2.4 The Modular Multilevel Clamped Capacitor Converter (MMC3)

The MMC3 can be viewed as an improved Dickson converter with all active power devices, i.e., MOSFETs or IGBTs, as shown in Fig. 2.6 [39]. Bi-directional power flow can be realized for the MMC3 due to the use of active power switches, which is desirable in ap-

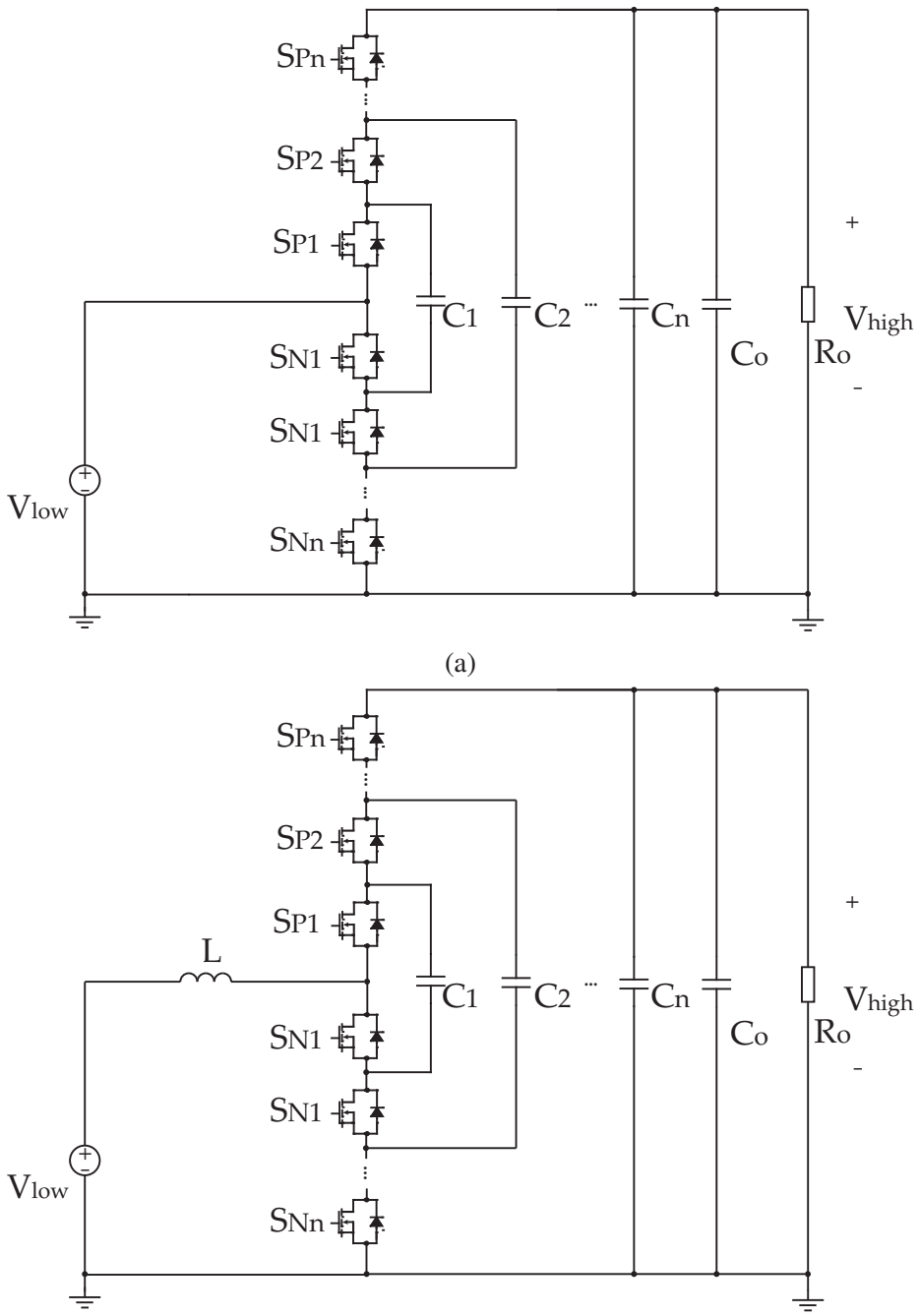


Figure 2.4: Circuit diagrams of an n-level (a) FCMDC and (b) FCML converter.

plications like HEV power management and Uninterruptable Power Supply (UPS) systems [3, 45]. Due to its modular structure as shown in Fig. 2.6, the MMC3 can conceptually meet any voltage level requirement with power switches rated at only 1 or 2 times of the low-side voltage, which is the same as the Dickson converter [5]. The MMC3 topology

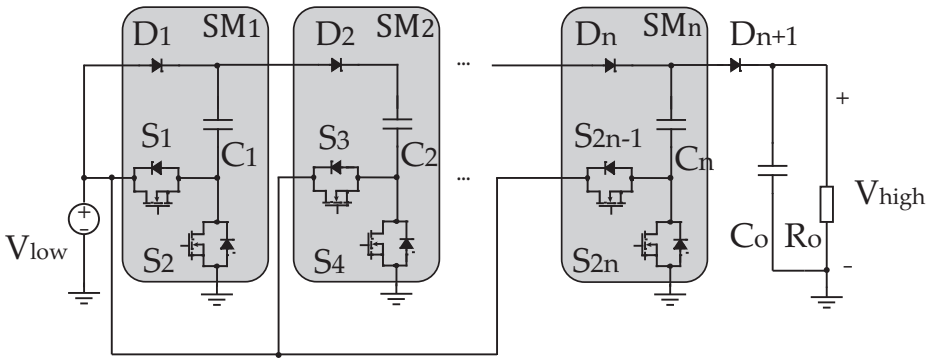


Figure 2.5: Circuit diagrams of an $(n+1)$-level Dickson converter.

also allows the bypass of failed SMs without disturbing its normal operation, which greatly enhances the reliability of the system [6].

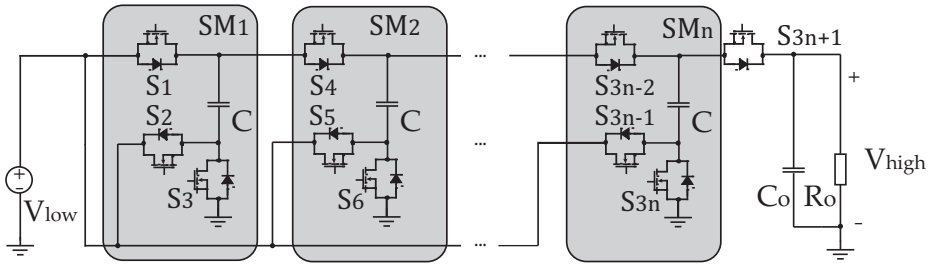


Figure 2.6: Circuit diagrams of an $(n+1)$-level MMC3.

Compared with the FCMDC and the FCML, the MMC3 also has several advantages. First of all, the MMC3 only has two switching states in open-loop operation regardless of its conversion ratio, which greatly enhances the scalability and reliability of the system. Secondly, the MMC3 has reduced conduction losses when its voltage-gain ratio is high since there are at most 3 switches conducting during any state, while there are n switches conducting during every state in the FCMDC [39]. The turn-off currents for the switches in the MMC3 during open-loop operation are the same as the load current, which are n times smaller than those for switches in the FCMDC, leading to significant reduction in switching losses [39]. The MMC3 also has better utilization of power transistors compared with the FCMDC as shown in [45] by having a lower total average VA stress for all transistors under the same input/output voltages and output power.

Despite the aforementioned features, the application of the MMC3 is still limited in power electronic systems due to several issues. First of all, the MMC3 lacks accurate and flexible output voltage control which could allow the system to 1) achieve continuously variable CRs and track an arbitrary output voltage reference within the achievable range and 2) maintain the output voltage under both input- and output-side disturbances/transients. Traditionally, the output voltage of the MMC3 can be only integer multiples/aliquots of the input voltage and the CR is not variable. The existing open-loop MMC3 cannot stabilize the output voltage when subjected to any transients/disturbances either in the source or output load [12]. Besides, large current spikes happen in the traditional MMC3 when capacitors with unbalanced voltages are connected in parallel, which leads to additional losses and component stresses [4]. The traditional MMC3 also suffers from discontinuous input current caused by charging/discharching of the capacitors, which is undesirable for the input voltage source.

To tackle these issues, resonant MMC3/Dickson converter topologies and new control methods have been proposed and studied. A resonant Dickson converter topology is proposed in [4, 46, 47], where an inductor is introduced at the low-voltage side to achieve continuous input current and ZCS for the power switches. A split-phase control method is also proposed to eliminate the current spikes during capacitor charging/discharging. However, closed-loop output voltage regulation cannot be realized at the same time due to the current-based control. A phase-shift control strategy is proposed in [48] and [49] to enable output voltage regulation and zero voltage switching for resonant MMC3. However, the complexity of both the topology and its control is increased, which greatly offsets the modularity and scalability of the MMC3. An asymmetrical (n/m)X MMC3 is proposed in [50], which can realize all natural-number CRs. However, the CR cannot be varied continuously and is limited to discrete numbers. Thus, the output voltage cannot be controlled to track any specific reference value and regulated dynamically in the event of input- or load-side transients.

On the other hand, with a modular structure, identical SMs can be inserted/bypassed during operation of the MMC3 in order to vary its CR or bypass/replace any faulty SMs to maintain its normal operation [6]. However, the insert/bypass action described in [6] will create large gaps between SM capacitor voltages, leading to significant current spikes during the transient that may cause over-current failures in the power devices. In addition, the insert/bypass operation has not been studied for the MMC3 with closed-loop control or inductive components for resonant operation. Thus, a procedure to reliably insert/bypass SMs of the MMC3 with inductive components and under various control schemes is needed.

2.5 Conclusion

Conventional switch-mode power converters are not suitable for applications that require high voltage gains due to presence of bulky inductive components, extreme duty ratios and overrated power devices. Various SC DC-DC converter topologies have been proposed to address these problems, among which the MMC3 demonstrates significant advantages including low stress on its power devices, reduced power losses, simple control implementation, bi-directional power flow and enhanced scalability and reliability with its multilevel and modular structure. However, to fully exploit the advantages of the MMC3, an accurate and flexible output voltage control is needed, and other technical challenges, including reducing large current spikes and achieving reliable insert/bypass of SMs, must be addressed.

CHAPTER 3
POWER LOSS ANALYSIS OF POWER ELECTRONIC SYSTEMS

Power loss analysis is an important part during the design of power electronic systems. In this chapter, basic methods to calculate power losses for power devices, passive components including capacitors, inductors and transformers are intorduced. These methods are used to analyze and compare power losses of the Modular Multilevel Converter (MMC) as a case study, and are also used in other chapters of this work for power loss analysis.

3.1 Power Device Loss Analysis

The power devices, including power switches and diodes, generally contribute to the major portion of power losses in the system. The power losses associated with power devices include both conduction loss and switching loss.

3.1.1 Conduction Loss

The conduction loss of a power device can be obtained by multiplying the current through the device and the corresponding voltage drop, which are mostly available in device datasheets. To obtain an approximate fomula to calculate the conduction loss $P_{T,\mathrm{cond}}$ from the instantaneous current i_d, a polynomial fitting curve is developed in the form of

$$P_{T,\mathrm{cond}} = a(T_j)i_d^2 + b(T_j)i_d + c(T_j), \tag{3.1}$$

3.1.2 Switching Loss

To calculate the switching losses, the switching-loss factors are defined as [51]

$$k_{\mathrm{ON}}(i_d, T_j) = \frac{E_{\mathrm{ON}}}{i_d}, \tag{3.2a}$$

$$k_{\mathrm{OFF}}(i_d, T_j) = \frac{E_{\mathrm{OFF}}}{i_d}, \tag{3.2b}$$

where E_{ON} and E_{OFF} are the turn-on and turn-off switching loss energy, respectively. These loss energy profiles are also available in most device datasheets. Based on (3.2), the switching loss energy is a function of drain current i_d and junction temperature T_j. The switching-loss factors (and thus the switching loss energy) can then be approximated by curve fitting in the form of

$$k_{\mathrm{ON}}(i_d, T_j) = a_{\mathrm{ON}}(T_j) i_d^2 + b_{\mathrm{ON}}(T_j) i_d + c_{\mathrm{ON}}(T_j), \tag{3.3a}$$

$$k_{\mathrm{OFF}}(i_d, T_j) = a_{\mathrm{OFF}}(T_j) i_d^2 + b_{\mathrm{OFF}}(T_j) i_d + c_{\mathrm{OFF}}(T_j). \tag{3.3b}$$

The switching energy losses can be estimated by

$$E_{\mathrm{T,ON}} = k_{\mathrm{ON}}(i_d, T_j) i_d \frac{v_{ds,\mathrm{B}}}{V_{ds,\mathrm{ref}}}, \tag{3.4a}$$

$$E_{\mathrm{T,OFF}} = k_{\mathrm{OFF}}(i_d, T_j) i_d \frac{v_{ds,\mathrm{B}}}{V_{ds,\mathrm{ref}}}, \tag{3.4b}$$

where $v_{ds,\mathrm{B}}$ represents the real-time blocking voltage and $V_{ds,\mathrm{ref}}$ is the blocking voltage under which the energy-current relationship is obtained. A similar method is applied to calculate the reverse-recovery energy loss of the power diode.

The total switching losses are calculated as the summation of all switching on/off en-

ergy losses within an interval

$$P_{\mathrm{ON}} = \frac{1}{t_1 - t_0} \sum (E_{\mathrm{T,ON}}), \tag{3.5a}$$

$$P_{\mathrm{OFF}} = \frac{1}{t_1 - t_0} \sum (E_{\mathrm{T,OFF}}). \tag{3.5b}$$

The total losses of a device are the summation of its conduction and switching losses as well as the conduction loss of its anti-paralleled diode, given by

$$P_{\mathrm{TOTAL}} = P_{T,\mathrm{cond}} + P_{D,\mathrm{cond}} + P_{\mathrm{ON}} + P_{\mathrm{OFF}}. \tag{3.6}$$

3.1.3 Soft-switching Techniques

In order to reduce the size of passive components and/or improve harmonic/ripple performance of power electronic systems, increased switching frequency is often desired. However, switching loss can become dominant and lead to requirement for overrated devices. Wide Bandgap (WBG) devices such as SiC and GaN power devices are favorable due to fast switching speed, which helps to reduce the switching loss. However, the fast switching transitions also lead to problems such as cross-talk [23] and high Electro-Magnetic Interference (EMI) noise. Thus, soft-switching techniques are needed to reduce switching loss and deal with problems related to fast-switching.

There are mainly two soft-switching techniques used in power electronic circuits, namely Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS). ZVS is achieved by switching the power device while its blocking voltage is zero. This is normally achieved by turning-on or off the power device while current is flowing through its body diode. ZCS is achieved when there is no current flowing through the device at the switching transient. It is mainly achieved by utilizing the resonant network formed by external inductors, capacitors as well as parasitic inductance/capacitance in the circuit and turning on/off the power device when the current is zero.

Switching loss of the power device is greatly reduced by either soft-switching technique and thus can be ignored in loss analysis. However, additional losses may need to be accounted for under certain conditions. For ZCS operation, during device turn-off, the parasitic output capacitance will be charged to the blocking voltage. This process generally involves no additional power loss as the charging current will not go through the channel of device. However, during the next turn-on, even when there is no current flowing through the device, the output capacitance will discharge through the channel, which contributes to switching loss. Thus, for device under ZCS operation, the switching loss should be considered as

$$P_{sw} = V_{block} Q_{OSS} f_{sw}, \tag{3.7}$$

where V_{block} is the blocking voltage when the device is off, Q_{OSS} is the output charge of the device, and f_{sw} is the switching frequency.

On the other hand, for ZVS operation, when the current is flowing through the body diode of device at turn-on, there is no additional switching loss. However, if the body diode is conducting current when device is turned-off, and the current does not decrease to zero before transferring to another path, there will be significant loss due to the reverse recovery of the body diode which can lead to damage of power devices. Thus, ZVS turn-off utilizing the body diode is not recommended in most cases.

3.1.4 Gate Drive Losses

The gate drive losses consist of losses associated with device gate charge, gate resistors as well as gate driver ICs, level shifters and auxillary power supplies. The gate charge loss can be estimated by

$$P_{gate} = V_{drive} Q_g f_{sw}, \tag{3.8}$$

where V_{drive} is the gate driver output voltage when turning the device on and Q_g is the gate charge of the device.

The gate resistor loss needs to be calculated for both turn-on and turn-off as different resistor networks may be used to reduce cross-talk effect [23]. Here, a MOSFET is used as an example for illustration. In order to calculate the gate current accurately, a detailed model for a MOSFET turn-on/off process as in [25] is used. During the turn-on of the device, there are three phases. During phase one, the gate drive voltage is applied to the RC network formed by the gate resistor and gate-source capacitance of the device, and gate current can be described as

$$i_{gate}(t) = \frac{V_{drive}}{R_{gate}} e^{\frac{-t}{R_{gate}C_{gs}}}. \tag{3.9}$$

After the device's gate voltage reaches threshold, the channel is open and the drain-source voltage V_{ds} starts to fall quickly, and a significant current is drawn from the gate current to charge C_{gd}. The device enters Miller plateau when

$$\frac{V_{drive} - V_{gs}}{R_{gate}} = C_{gd} \frac{-dV_{ds}}{dt}. \tag{3.10}$$

During this period, as all available gate current is charing C_{gd}, the gate-source voltage of device will remain constant, and the gate current is given by

$$i_{gate}(t) = \frac{V_{drive} - V_{gs}}{R_{gate}}. \tag{3.11}$$

Subsequent to V_{ds} drop, the gate current is again available to charge C_{gs} to the full V_{drive}. The current in this phase will follow the same description as in equation (3.9). Based on the above analysis, the gate current RMS can be determined and gate resistor loss can be calculated. The analysis can be extended to the turn-off process as well.

The power loss associated solely with gate driver ICs, level shifters and auxillary power supplies are minimal compared with the above losses and very complicated to determine.

Thus, only the losses associated with device gate charge and gate resistors are taken into account in this work.

3.2 Passive Component Power Loss Analysis

Another important source of power loss is from the passive components in the circuit, i.e., inductors, capacitors and transformers. For capacitors, the major power loss comes from their Equivalent Series Resistance (ESR), which generates ohmic loss during charging and discharging. The power loss associated with capacitor can be calculated as

$$P_{cap} = nI_{cap}^2 R_{ESR}, \tag{3.12}$$

where n is the number of times the capacitor gets charged or discharged during one switching cycle and I_{cap} is the RMS current going through the capacitor.

The same method could be used to analyze power losses associated with inductors and transformers in the circuit as well. Besides the copper loss, these magnetic components also have core loss, which can be calculated according to the Steinmetz's equation as [52]

$$P_{core} = kf^a B^b, \tag{3.13}$$

where k, a and b are Steinmetz coefficients, f is the operating frequency and B is the maximum magnetic flux densigy. Another popular method to evaluate power losses of magnetic components is through their design process using the K_g method [53]. The K_g design method helps designer to select a proper magnetic core for the inductor or transformer based on peak magnetizing current and RMS current to satisfy a certain limit of copper and core losses. Through this design process, the copper and core losses of the inductor or transformer at full load can be determined and used directly in loss analysis.

3.3 Power Loss Analysis of the MMC: A Case Study

3.3.1 Basics of Operation of an MMC

The circuit diagram of a three-phase MMC is shown in Fig. 3.1(a). The MMC consists of two arms per each phase where each arm comprises n series-connected, nominally identical, half-bridge submodules (SMs), and a series-connected inductor.

Each SM of the MMC of Fig. 3.1 consists of a capacitor and a half bridge cell where its output voltage (i.e., V_{SM}) is either equal to its capacitor voltage (SM switched on/inserted) or zero (SM switched off/bypassed), depending on the corresponding switching state selected by the modulator. There are two complimentary switch pairs in each SM (i.e., S_1 and S_2). In the MMC of Fig. 3.1, the switching functions of the SMs of phase $j = a, b, c$ are controlled so that at any instant n SMs out of the $2n$ SMs of phase j are on (i.e., n_{upj} SMs in the upper arm and $n_{lowj} = n - n_{upj}$ in the lower arm). The values of n_{upj} and n_{lowj} are in the range of zero to n and are determined by the desired ac-side voltage level of phase j [54]. In principle, each MMC arm represents a controllable voltage source, i.e., v_{upj} (the sum of the output voltages of the switched-on SMs in the upper arm) and v_{lowj} (the sum of the output voltages of the switched-on SMs in the lower arm), as depicted in Fig. 3.1.

Assuming that each SM capacitor voltage is ideally regulated at V_{dc}/n, an ideal $(n+1)$-level waveform, with respect to the dc-side midpoint O, at the ac-side terminal of phase-j of the MMC is synthesized and formulated as

$$v_{tj} = \frac{n_{\mathtt{low}j} - n_{\mathtt{up}j}}{2n} V_{dc}, \tag{3.14}$$

where $v_{tj}, j = a, b, c$, is the ac-side voltage of the MMC. As $n_{\mathtt{up}j}$ and $n_{\mathtt{low}j} \epsilon \{0, 1, ..., n\}$ and $n_{\mathtt{up}j} + n_{\mathtt{low}j} = n$, based on (3.14), v_{tj} varies stepwise in the range of $V_{dc}/2$ to $-V_{dc}/2$ with a step size of V_{dc}/n, as could be seen in Fig. 3.2. In practice, the capacitor voltages of the individual SMs of the MMC should be monitored and maintained balanced at their

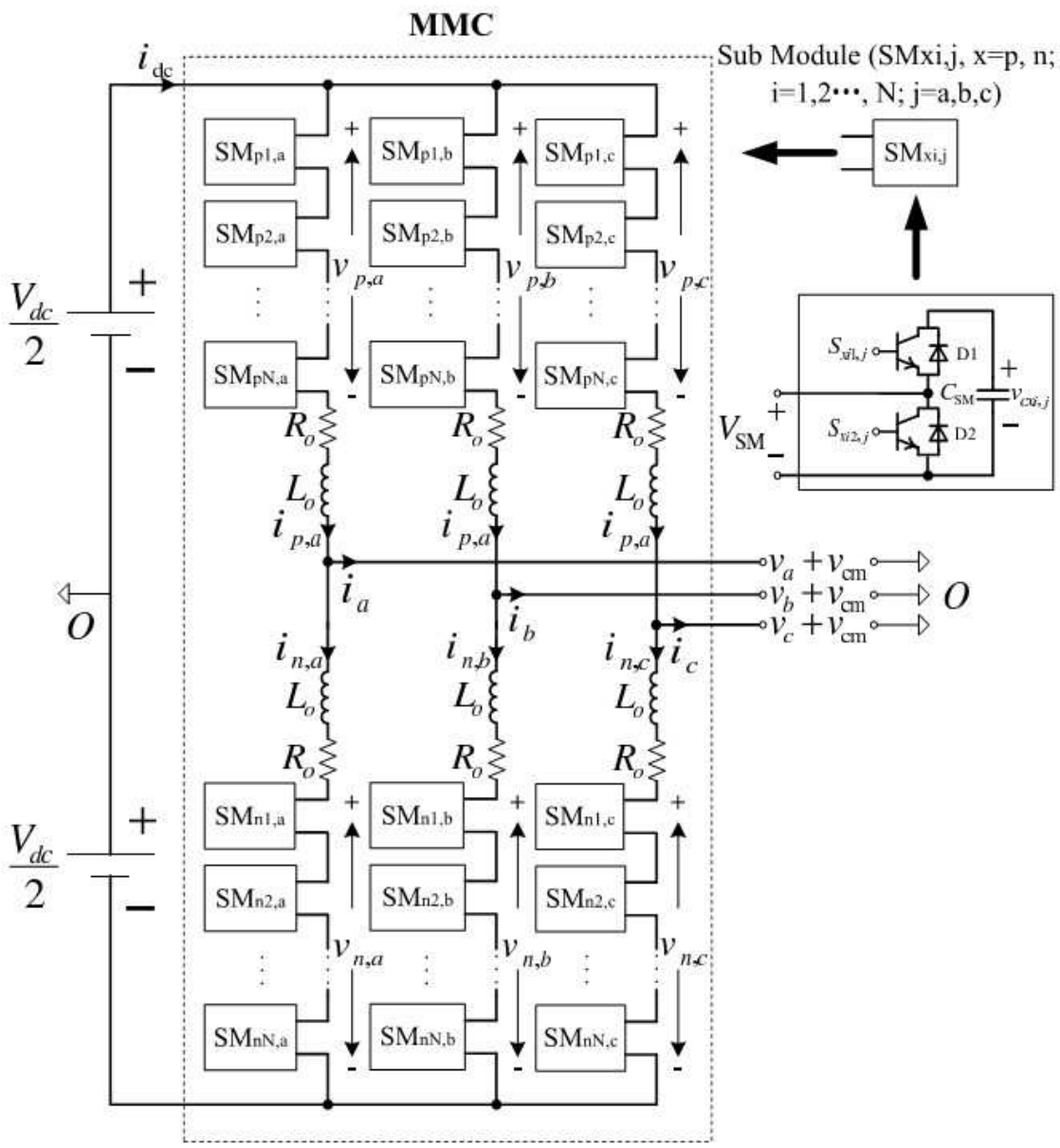


Figure 3.1: The MMC circuit diagram

nominal values, i.e., V_{dc}/n, by using an active voltage-balancing technique [55].

Representing the ac-side current by i_j, the corresponding arm currents are described by

$$i_{\mathrm{up}j} = \frac{i_j}{2} + \frac{i_{dc}}{3} + i_{zj}, \tag{3.15a}$$

$$i_{\mathrm{low}j} = -\frac{i_j}{2} + \frac{i_{dc}}{3} + i_{zj}, \tag{3.15b}$$

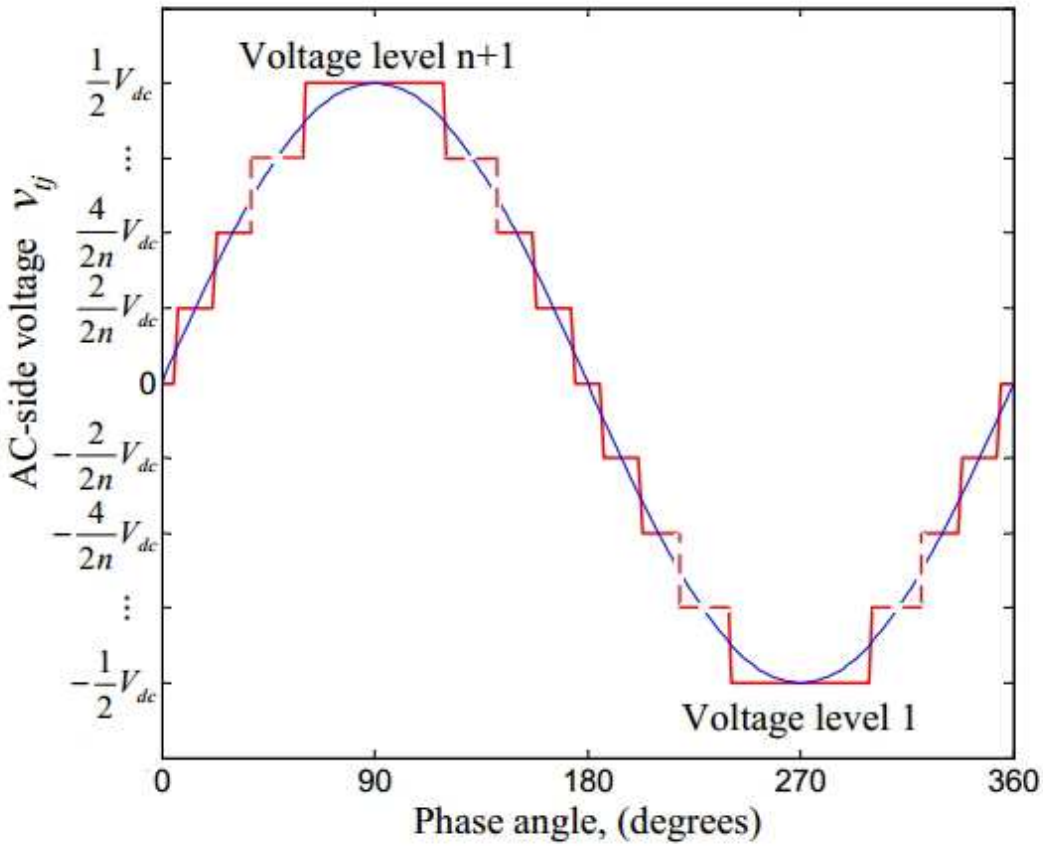


Figure 3.2: Typical ac-side MMC output voltage waveform.

where i_{zj} represents the circulating current flowing through phase j [56]. Circulating currents flowing through the three phase legs of the MMC originate from the voltage differences among the phase legs [57], [58] and contain negative sequence components with the frequencies twice the fundamental one [58]. Circulating currents do not have any impact on the ac-side voltages and currents. However, if not properly controlled/suppressed, they increase (i) the peak and rms values of the phase-leg currents, which consequently increase the converter power losses, (ii) the magnitude of the SM capacitor voltage ripple, and (iii) the size of the converter components. Although proper sizing of the arm inductors can suppress the circulating currents to some extent [57], a circulating current controller technique is necessary to effectively control/suppress them [57].

Due to its scalability and modularity, by stacking up sufficient number of SMs based

on commercially available semiconductor devices, the MMC can conceptually meet any voltage level requirement. The MMC has been widely accepted/investigated for HVDC transmission systems where the SMs are realized based on Si semiconductor devices, i.e., IGBTs and their anti-parallle diodes. One of the main concerns in the design, operation, and control of the MMC, particularly for high-power applications, is its efficiency [59]. As of now, improving the efficiency of the MMC has been mainly acheived by mitigating/reducing its circulating currents. Efficiency improvement of the MMC based on various SM circuits and semiconductor devices, e.g., IGBT and IGCT devices is reported in [15, 60]. Reference [15] investigates the possibility of using SiC JFETs for efficiency improvement of the MMCs. However, the analysis is based on the assumption of having high-voltage SiC JFETs, which is still far from reality.

3.3.2 Evaluation and Comparison of Power Losses

To evaluate and compare the efficiency of the MMC based on various semiconductor devices, a grid-connected MMC system is implemented in the PSCAD/EMTD software environment. The parameters of the system are listed in Table 3.1.

Table 3.1: Paremeters of the MMC Study System

MMC nominal power	500 kW
AC system nominal voltage	10 kV
Nominal frequency	60 Hz
DC nominal voltage	20 kV
No. of SMs per arm, N	20
SM capacitor voltage, V_c	1 kV
SM capacitance, C	3.3 mF
Arm inductance, L	15 mH

The voltage and current are measured and the switching transitions are recorded to calculate the power losses of each submodule and, consequently, the semiconductor losses of the MMC system. Two SiC MOSFETs and two Si IGBTs are characterized using information of their datasheets based on the methods introduced in Sections 3.1.1 and 3.1.2. By

combining the characterization results with voltages and currents of the MMC, the MMC power losses are calculated and compared. The summary of results is given in Table 3.2, where the conduction and switching losses are associated with one phase of the MMC, while the total loss percentage indicates the portion of overal MMC power losses at rated power. To compare the power losses under various operating conditions, the efficeincy of the MMC is calculated at 500 kW, 300 kW, and 200 kW.

Table 3.2: Summary of Power Losses ($T_j = 135\ ^oC$)

Device	P_{cond} (kW)	P_{switch} (kW)	P_{total} (%)	Nominal Power (kW)
CMF20120D	1.1537	0.0105	0.698	500
C2M0025120D	0.393	0.0097	0.241	500
Si IGBT 1	0.7836	0.0594	0.506	500
Si IGBT 2	0.8136	0.145	0.575	500
Anti-parallel diode	0.021	0	0.128	500
CMF20120D	0.420	0.006	0.426	300
C2M0025120D	0.126	0.005	0.131	300
Si IGBT 1	0.392	0.032	0.424	300
Si IGBT 2	0.389	0.091	0.480	300
CMF20120D	0.237	0.0038	0.362	200
C2M0025120D	0.063	0.003	0.100	200
Si IGBT 1	0.225	0.019	0.366	200
Si IGBT 2	0.222	0.058	0.420	200

In the case of MMC with 500 kW, the total power losses of CMF20120D SiC MOSFET are higher that those from Si IGBTs. The main reason is that the conduction losses of this SiC MOSFET is significantly larger. As shown in Table 3.2, the switching losses are only a small portion of the total losses, and the conduction losses are dominant. This is due to the low switching frequency of the MMC as listed in Table 3.2. Therefore, although the switching losses of CMF20120D SiC MOSFET is much smaller than its Si conterparts, its high conduction losses overshadow its advantages. In the 300-kW case, however, as the difference in conduction losses becomes smaller, the total power losses of CMF20120D SiC MOSFET become smaller than those of Si IGBT 2 and very close to that of Si IGBT 1. In the 200-kW case, CMF20120D SiC MOSFET losses become smaller than those

from both Si IGBTs. On the other hand, compared to CMF20120D SiC MOSFET, the switching losses of C2M0025120D SiC MOSFET are significantly lower. C2M0025120D SiC MOSFET has a smaller on-state resistance, i.e., 25 mΩ, which leads to noticeably reduced conduction losses. Its switching losses are also much smaller than Si IGBTs and slightly lower than CMF20120D SiC MOSFET.

The on-state characteristics, i.e., drain current vs. voltage drop, of all under-investigation devices at a junction temperature of 135 ^{o}C is shown in Fig. 3.3. Since the conduction losses are calculated as the product of the voltage drop and the drain current, for a given current, the higher the corresponding voltage drop is, the higher the conduction losses are. For the considered operating power levels, the current flowing through the devices is in the range of 0 to 24 A for the 500-kW case, 0 to 16 A for the 300-kW case, and 0 to 11 A for 200-kW case. Based on the range of current for different power levels, as shown in Fig. 3.3, with 24 A current and compared to the other devices, the C2M0025120D SiC MOSFET has the lowest voltage drop. This leads to the lowest conduction losses of C2M0025120D SiC MOSFET. For most of the operating current range, the characteristics of Si IGBT 1 and Si IGBT 2 are very close to each other, resulting in similar conduction losses. For currents below 12 A, CMF20120D SiC MOSFET has smaller conduction losses than the IGBTs, i.e., corresponding to the higher conduction losses for 500-kW and 300-kW cases, where currents are mostly above 12 A.

3.4 Conclusions

In this chapter, basic methods of power loss analysis in power electronic systems are introduced. A case study is carried out where power losses in MMC systems based on SiC and Si devices are compared. The study results conclude that, due to higher conduction losses of the commercially available SiC MOSFETs, the SiC-based MMC is less efficienct that the MMC based on Si IGBTs with the same specifications. Since the switching frequency of the SiC devices in the MMC are not high, the conduction losses are dominant

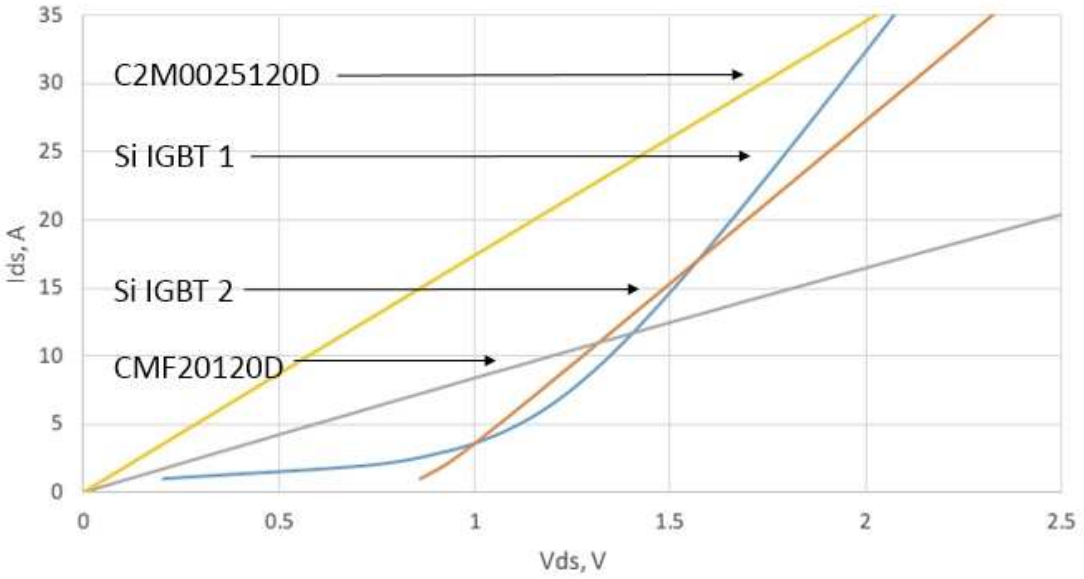


Figure 3.3: On-state characteristics of devices

loss component. SiC MOSFETs are suitable for applications in which the switching frequency is very high so their benefits in terms of power losses can be exploited. The power loss analysis methods introduced in this chapter are used throughout the rest of this work.

CHAPTER 4
ELECTRO-THERMAL MODEL OF GAN POWER DEVICES

As discussed in Chapter 2, the Wide Band-Gap (WBG) switching devices, particularly GaN devices, have become attractive switching devices for power electronic systems due to their unique electrical and thermal capabilities/characteristics compared to their Si counterparts. As the devices and power electronic systems become smaller, the heat dissipation becomes more difficult and new challenges are imposed on thermal management [10]. Therefore, at the design stage of GaN-based power electronic systems, it is necessary to determine the junction temperature profile of the switching devices to ensure that they operate within their safe operation area. The junction temperature also has significant impacts on the electrical performance of GaN FET devices, and therefore, for accurate temperature estimation, the device model needs to take the thermal impacts into account [30, 31]. Consequently, electro-thermal modeling of GaN devices is one of the important steps for system design/integration. However, to the best of the authors' knowledge, no behavioral electro-thermal model for circuit simulation that considers both device static and switching characteristics has been developed for GaN FETs.

In this chapter, a simple behavioral electro-thermal model for EPC2010C GaN FET is developed in the LTSPICE software environment. The model couples an available electrical model of the device with a thermal RC network to count the self-heating effects. The developed model embeds the impacts of junction temperature on the device static and switching characteristics by using a gate voltage modification circuit. The accuracy of the developed model is validated against the original fixed-temperature electrical model. To demonstrate the capability/accuracy of the developed model in estimating the junction temperature pro-

file of the device in the SPICE circuit simulation, a boost converter is used as the benchmark system. The simulation waveforms based on the developed model are compared with their experimental counterparts obtained from a Double Pulse Tester (DPT) circuit built based on EPC2010C GaN FETs, and the thermal measurement of an EPC2010C GaN FET operating in a boost converter.

4.1 The Proposed Electro-thermal Model of the GaN FET

In general, an electro-thermal model consists of an electrical model of the device coupled with a thermal RC network [30, 61]. The thermal network, as shown in Fig. 4.1, takes the dissipated power in the device as the input and provides the voltage across the network, which represents the junction temperature, as the output. The junction temperature is fed back into the electrical model, impacting the device parameters and characteristics. Although the available electrical models have built-in functions to calculate device parameters at various junction temperatures, they are not capable of dynamically updating the parameters with a variable temperature profile during simulation. In this thesis, a gate voltage modification circuit is developed, which, as shown in Fig. 4.2(a), modifies the gate voltage of the device based on its junction temperature profile, thereby attaining an accurate electro-thermal model.

As shown in Fig. 4.2, three diodes are considered in each branch of the gate modification circuit, which ensure the gate current flows in the expected direction. Furthermore, two switches S_1 and S_2 are turned on/off with optimal timing to complete the gate voltage modification during device conduction period and switching transients, respectively. To minimize the impacts on the device performance during the SPICE simulation, ideal diodes with no forward voltage drop have been used. S_1 and S_2 are ideal switches with voltage across the GaN switch as the control signal. If the voltage across the GaN switch falls below 0.3 V, the switch is identified to be operating in the conduction mode and S_1 conducts while S_2 is blocked. If the voltage is beyond 0.3 V, the GaN switch is identified in

the switching transition mode and S_2 conducts while S_1 is blocked. The dissipated power P_{diss} is modeled as a controlled current source whose value is calculated as the product of the device voltage and current.

The operating principles and implementation of the modification circuit applied to the gate terminal are explained in details in the following sections.

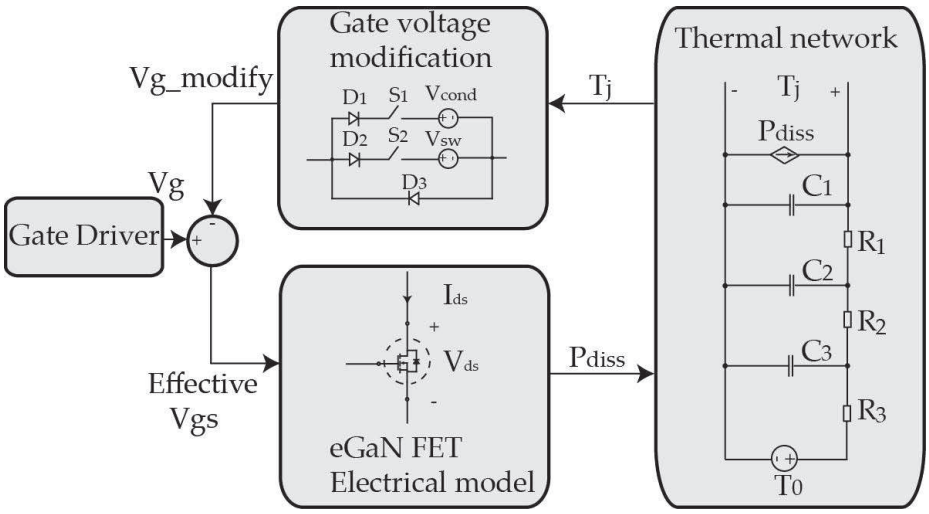


Figure 4.1: Block diagram of the proposed electro-thermal model.

4.1.1 Modeling of Static Characteristics

The key parameter for the static characteristic of the device, which refers to I_{ds}-V_{ds} relationship during conduction period, is the on-state resistance, $R_{ds,on}$. The on-state resistance of GaN FET is a near-linear function of its junction temperature as shown in Fig. 4.3 (b) [62]. On the other hand, at fix-temperature simulations of the circuit in Fig. 4.3(a), $R_{ds,on}$ is also found to be a function of the gate voltage V_{gs}, as shown in Fig. 4.3(b). Thus, by using an additional voltage source V_{cond} controlled by the junction temperature during conduction period as shown in Fig. 4.2(b), $R_{ds,on}$ can be changed based on the junction temperature profile. The value of V_{cond} is determined by a look-up table reflecting $R_{ds,on}$-V_{gs} relationship obtained from Fig. 4.3(a) by applying several different gate voltages. During an electro-thermal simulation using the proposed model, first, the $R_{ds,on}$ corresponding to the

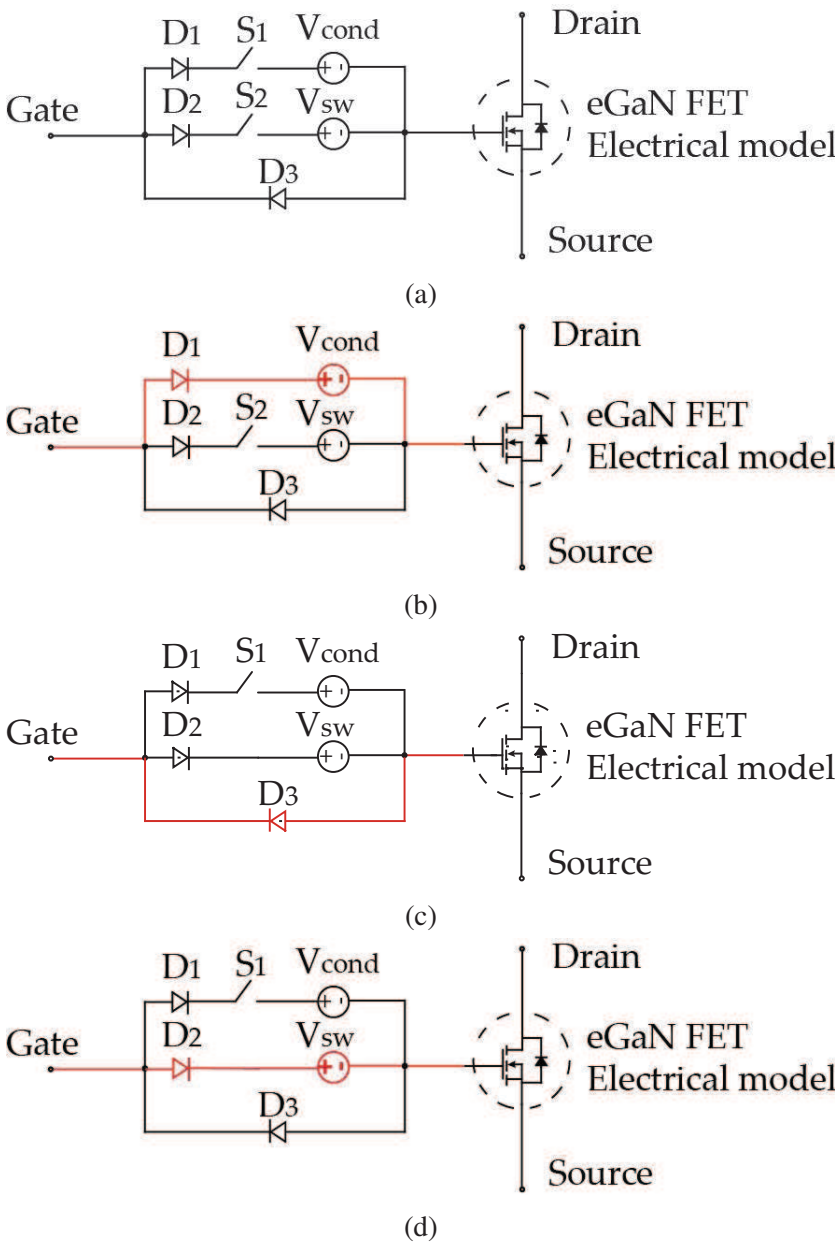
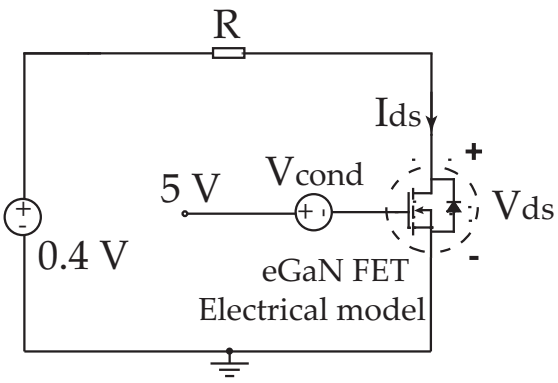
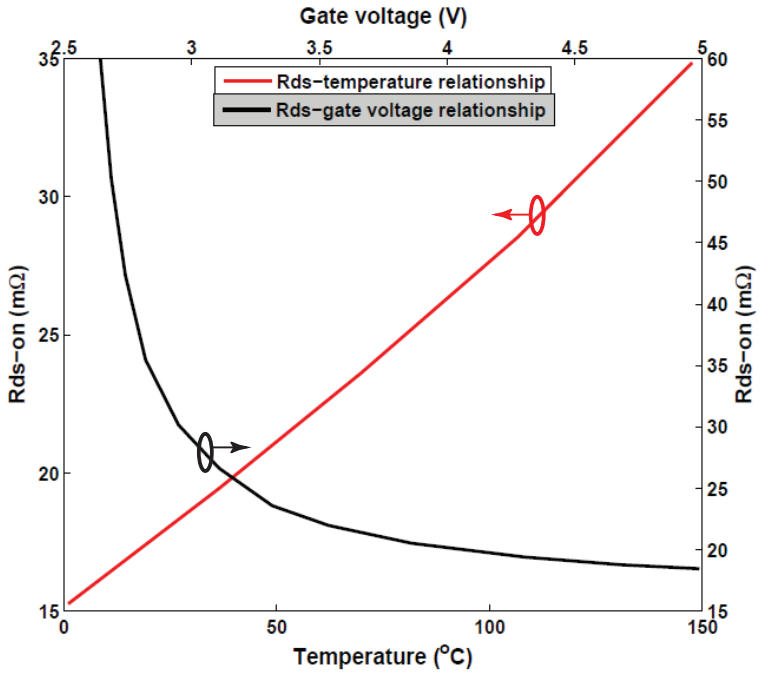


Figure 4.2: (a) The proposed gate voltage modification circuit and (b), (c) and (d) its operation principles during device conduction period and turn-off and turn-on transients, respectively.

current temperature is calculated based on $R_{ds,on}$-temperature relationship, and an arbitrary behavioral voltage source in LTSPICE is used as V_{cond} with values determined based on the $R_{ds,on}$-V_{gs} look-up table.



(a)



(b)

Figure 4.3: (a) Circuit to test $R_{ds,on}$-V_{gs} relationship and (b) relationship between the on-state resistance, junction temperature and gate voltage.

4.1.2 Modeling of Switching Characteristics

To model the temperature-dependent switching characteristics of the device, the impacts of junction temperature on the device turn-off and turn-on transients need to be identified. By using a conventional DPT circuit as in Fig. 4.4 in the LTSPICE environment, it is observed that the turn-off transient is almost independent of junction temperature, while $\frac{dV_{ds}}{dt}$ during

the turn-on transition has a near-linear relationship with the junction temperature. Thus, during turn-off transition, the device is connected directly to the gate driver through the diode D_3, as shown in Fig. 4.2(c). During turn-on transition, $\frac{dV_{ds}}{dt}$ is determined by [25]:

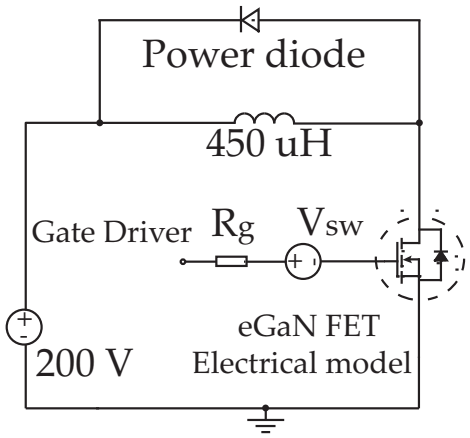


Figure 4.4: The DPT circuit used in simulation.

$$\frac{dV_{ds}}{dt} = -\frac{V_{gs,on} - V_{plateau}}{R_g C_{gd}}, \tag{4.1}$$

where V_{ds} is the drain-source voltage, $V_{gs,on}$ is the turn-on voltage provided by the gate driver, $V_{plateau}$ is the Miller plateau voltage, R_g is the gate resistance and C_{gd} is the gate-drain capacitance of the device. Therefore, by using an additional voltage source V_{sw} in the gate loop during the turn-on transient as shown in Fig. 4.2(d), the effective $V_{gs,on}$ of the device can be modified. This, accordingly, changes $\frac{dV_{ds}}{dt}$. To determine the value of V_{sw} for a given temperature, V_{sw} is varied in the circuit simulation in Fig. 4.4 under 25 ^{o}C until the $\frac{dV_{ds}}{dt}$ becomes the same with that under the given temperature. A look-up table reflecting V_{sw}-temperature relationship is built by repeating this process. An arbitrary behavioral voltage source in LTSPICE is used as V_{sw} with values determined based on the V_{sw}-temperature look-up table.

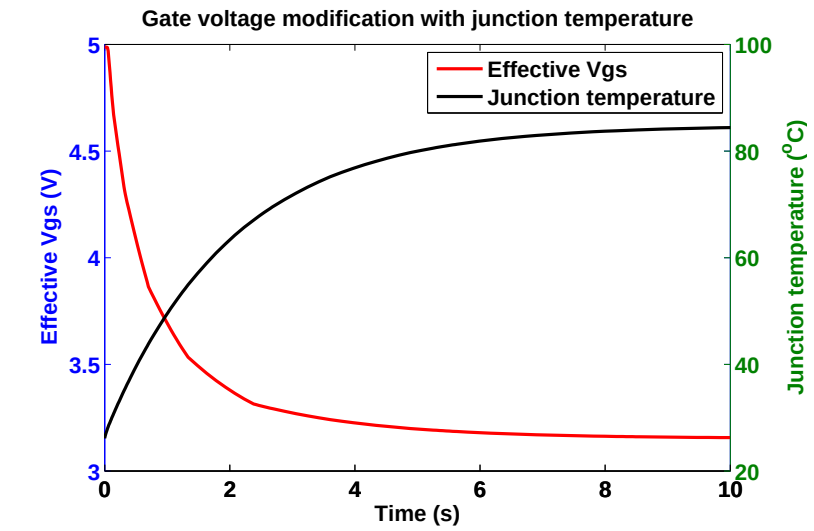
4.2 Model Validation

4.2.1 Static Characteristic

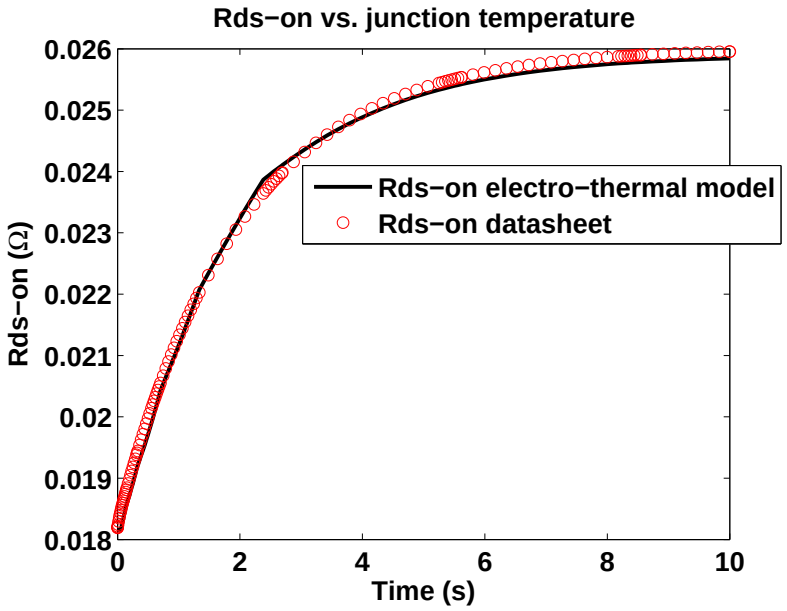
To validate the temperature-dependent static characteristic, the developed model is coupled with a time-varying temperature profile generated from a constant power source and a thermal RC network derived from the device datasheet [62], being under DC bias to extract the on-state resistance. As shown in Fig. 4.5(a), the effective gate-source voltage observed by the electrical device model is changed according to the varying junction temperature, and the modeled on-state resistance is consistent with the resistance estimated based on datasheet throughout the time period as in Fig. 4.5(b).

4.2.2 Switching Characteristics

For switching transients, the developed model is implemented in a DPT circuit at various fixed temperatures, assuming that the time constant of the thermal system is sufficiently large so the temperature remains constant during a switching event [35]. The drain-source voltage V_{ds} and current I_{ds} waveforms during switching transients are shown in Fig. 4.6 at a junction temperature of 85 ^{o}C. By comparing the switching characteristics of the device based on the original electrical model at 25 ^{o}C and 85 ^{o}C, the impacts of junction temperature on the switching characteristics can be observed in Fig. 4.6. As shown in Fig. 4.6(a), the estimated turn-off transient of the device based on the developed model at 85 ^{o}C is similar to the one from the original electrical model. The estimated turn-on transient of the device is also closely matched with the one from the original electrical model. Nevertheless, the overshoot current waveform of I_{ds} during the turn-on transition is not modeled quite accurately because under fixed-temperature simulation, the simulation temperature also impacts other devices such as diodes in the circuit while the proposed electro-thermal model only accounts for the GaN FET. However, the accuracy of the developed model is illustrated by $\frac{dI_{ds}}{dt}$ prior to the overshoot and the end of turn-on transient.



(a)

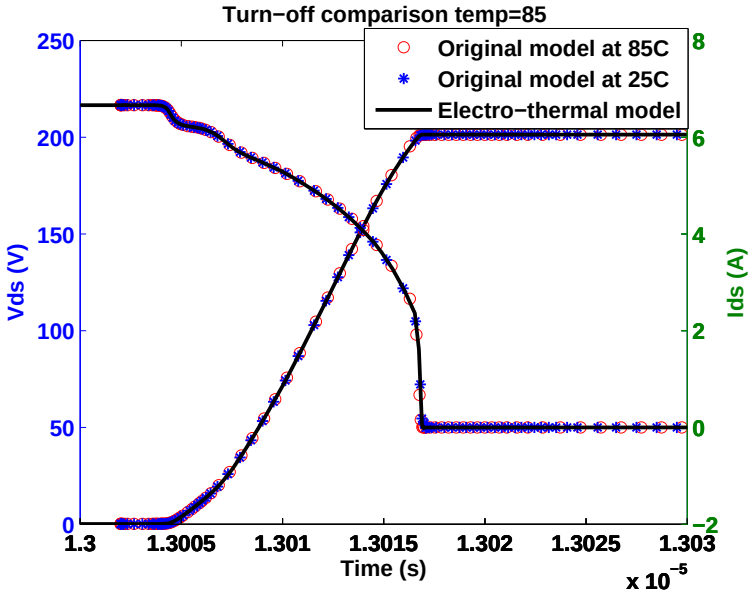


(b)

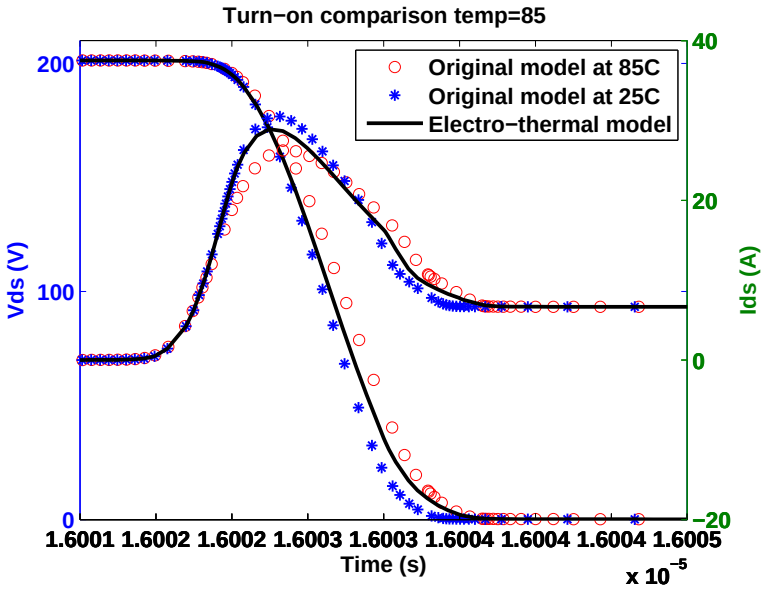
Figure 4.5: (a) Gate voltage modification of the electro-thermal model during conduction mode with the junction temperature profile and (b) the modeled temperature-dependent on-state resistance and the resistance calculated based on datasheet.

4.2.3 Gate Voltage and Current

One consideration in the development of the proposed model is to have minimal impacts on the outer circuit while being capable of electro-thermal modeling. The gate voltage and current supplied by the gate driver are important factors that should not be interfered by



(a)



(b)

Figure 4.6: (a) Turn-off and (b) turn-on switching transients.

the developed device model. Thus, it is desired that the gate voltage and current viewed from the gate driver side remain the same for the developed model as well as the original one. To explore the impact of gate voltage modification circuit on the gate voltage and current, the gate voltage and current at the gate driver terminal are recorded from the DPT circuit simulation in Fig. 4.4 and compared with those obtained with the original model

at 85 ^{o}C, as shown in Fig. 4.7. The turn-off gate voltage and current are the same with original model as shown in Figs. 4.7(a) and (b). As shown in Figs. 4.7(c) and (d), there are differences in the gate voltage and current caused by the gate voltage modification circuit during the turn-on transient. However, the differences are very limited in terms of both amplitude and pattern of the waveforms, and thus does not induce much influence into the analysis.

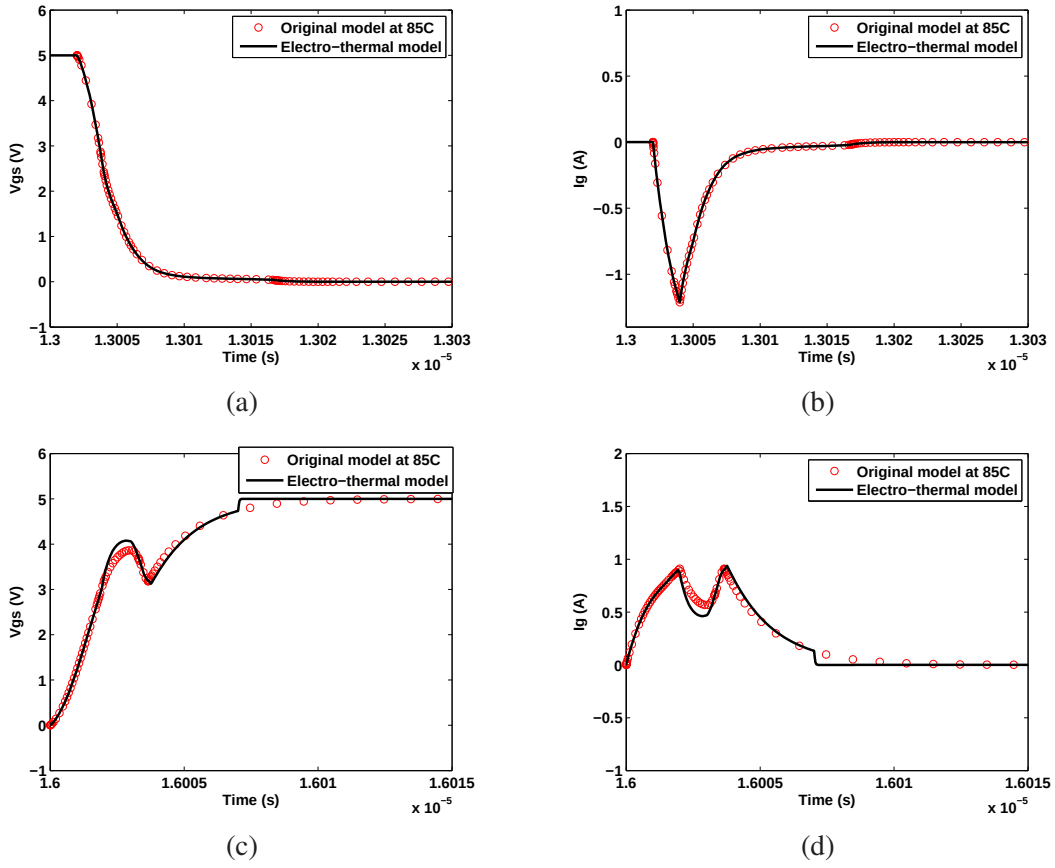


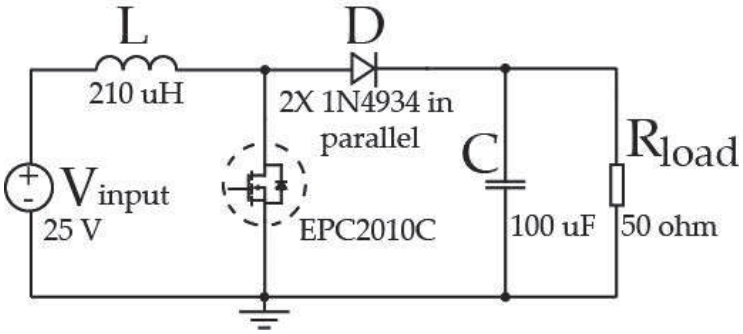
Figure 4.7: (a) and (b) Turn-off gate voltage and current and (c) and (d) turn-on gate voltage and current at 85 ^{o}C.

4.2.4 Circuit Simulation

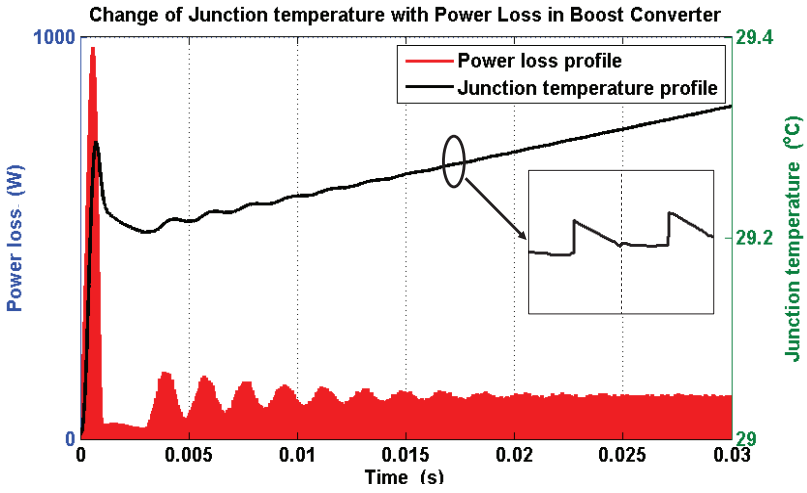
To demonstrate performance of the developed model for circuit simulation studies, a 25-50 V boost converter operating at 100 kHz is constructed in the LTSPICE software environment, using the developed electro-thermal model for the main switch, as shown in

Fig. 4.8(a). The coupled thermal RC network is developed based on the thermal SPICE model provided by EPC [63]. The power loss profile of the main switch and the corresponding junction temperature variations during the first 30 ms of simulation time are shown in Fig. 4.8(b). As shown in Fig. 4.8(b), the developed model is capable of dynamically estimating the junction temperature transients during switching cycles.

In order to measure the simulation speed, the time to run the same boost converter simulation for 3000 cycles at 100 kHz with and without the developed model is recorded. With the developed model implemented, the simulation time is about 1 minute, while the simulation time with only the original model is 26.71 seconds, both with a PC using Intel 3.40 GHz processor with 16 GB RAM.



(a)



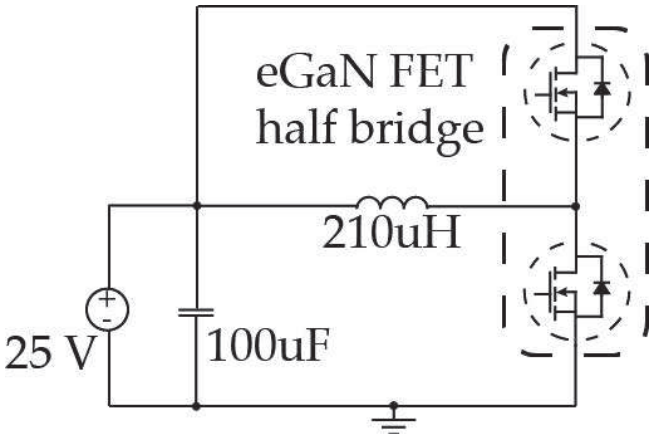
(b)

Figure 4.8: (a) The boost converter benchmark system and (b) junction temperature and power loss profile of the main switch based on the proposed electro-thermal model.

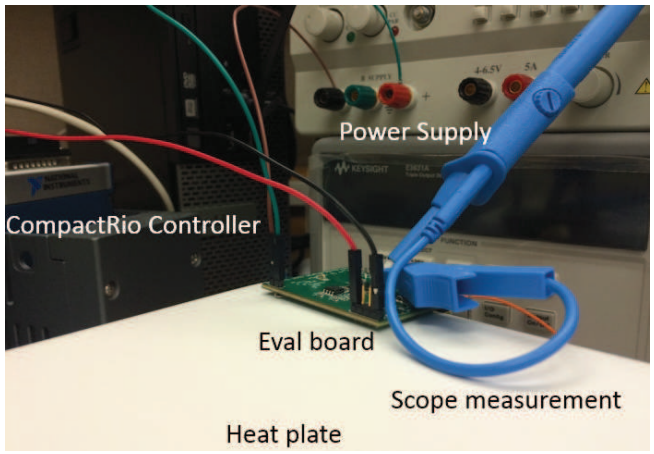
4.3 Experimental Validation

4.3.1 Switching Performance Validation

To validate the developed electro-thermal model with experimental results, a DPT circuit is built based on an EPC2010C half-bridge evaluation board from EPC shown in Fig. 7.2. The board is placed on a heatplate to conduct experiments under various controlled temperatures.



(a)



(b)

Figure 4.9: (a) Block digram and (b) experimental setup of the DPT circuit.

A comparison of the experimental and simulation results obtained with the developed electro-thermal model of V_{ds} of the lower switch at 50 ^{o}C during both turn-on and turn-off transients is presented in Figs. 4.10(a) and (b), and at 70 ^{o}C in Figs. 4.10(c) and (d), re-

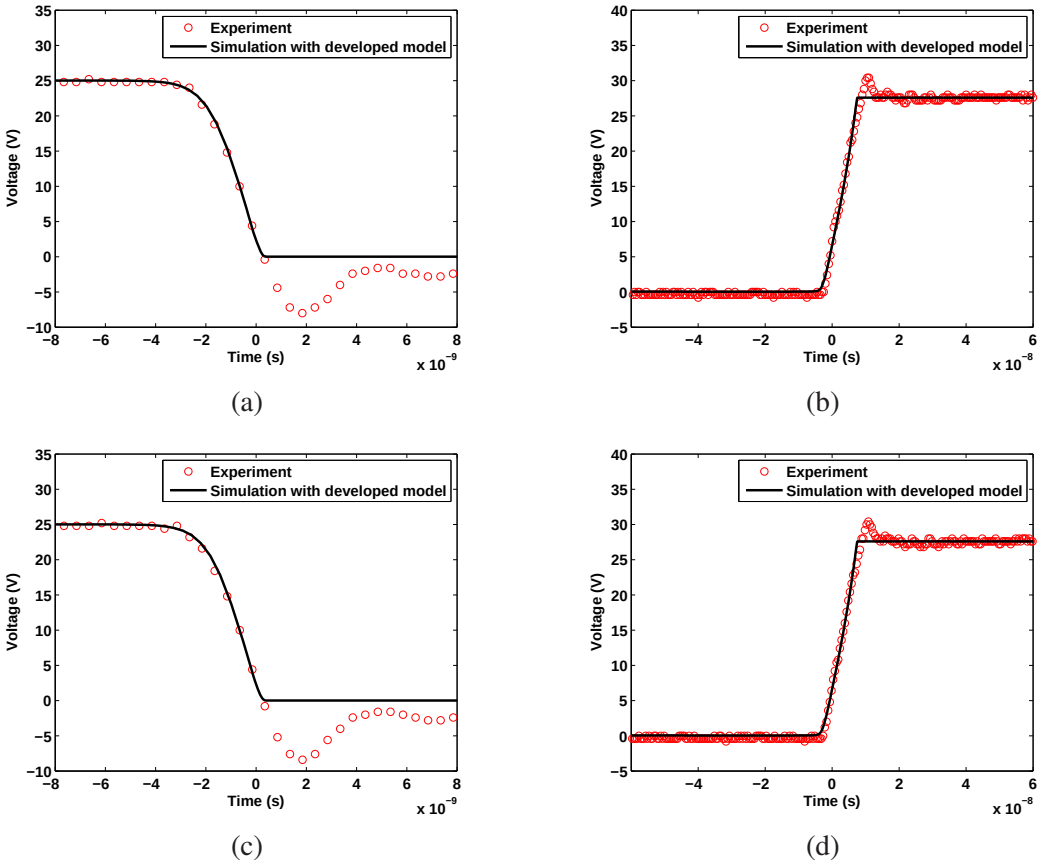


Figure 4.10: Comparison of experimental and simulation results of V_{ds} of the lower switch at 50 ^{o}C during (a) and (b) lower switch turn-on and turn-off transients, respectively, and at 70 ^{o}C during (c) and (d) lower switch turn-on and turn-off transients.

spectively. Based on Figs. 4.10(a) and (c), the simulated $\frac{dV_{ds}}{dt}$ during the transient is closely matched with the experimental result at different temperatures. On the other hand, the turn-off transient with the developed model also shows $\frac{dV_{ds}}{dt}$ that is close to the experimental result as in Figs. 4.10(b) and (d). However, the negative overshoot in V_{ds} present in the experimental result as observed in Figs. 4.10(a) and (c), as well as the positive voltage overshoot in Figs. 4.10(b) and (d), are not present in the simulation results. This is due to the circuit parasitics in the circuit [64], which are not included in this simulation.

In order to include the parasitics in the circuit simulation, the circuit parasitics estimated based on [64] have been added into the simulation as shown in Fig. 4.11. With the parasitics considered, the switching transients can be simulated more accurately as shown

in Fig. 4.12. The current through the device, which is experimentally measured under 50 ^{o}C and 70 ^{o}C and compared with its corresponding simulation result show in Figs. 4.13(a) and (b). Based on comparison, $\frac{dI}{dt}$ has been modeled very accurately and the simulated transients are very close to the experimental measurements. Current spikes can be observed in the simulation during the switching transients but are not present in the experimental measurement. This is mainly due to the limited resolution of current measurement devices that cannot follow the very fast transients of GaN devices.

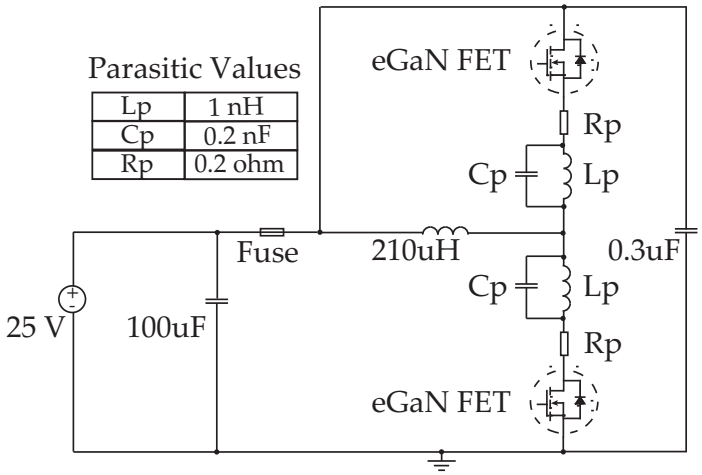


Figure 4.11: The DPT circuit simulation including parasitics.

4.3.2 Temperature Estimation Validation

To demonstrate the capability of the developed model in estimating the device temperature during circuit simulation and to compare the estimated result with experimental measurement, a boost converter system as in Fig. 4.14(a) is prototyped. The system runs for 5 minutes until the temperature settles down with the GaN FET operating at 500 kHz. The case temperature of the device is measured and recorded by an IR thermal imager as shown in Fig. 4.14. The measured data is then compared with the simulation result based on the developed electro-thermal model as in Fig. 4.15(a). In addition, an electro-thermal model for EPC2010C is developed in the PLECS toolbox based on device power losses at various temperatures obtained from LTSPICE simulation using the method in [65]. The same

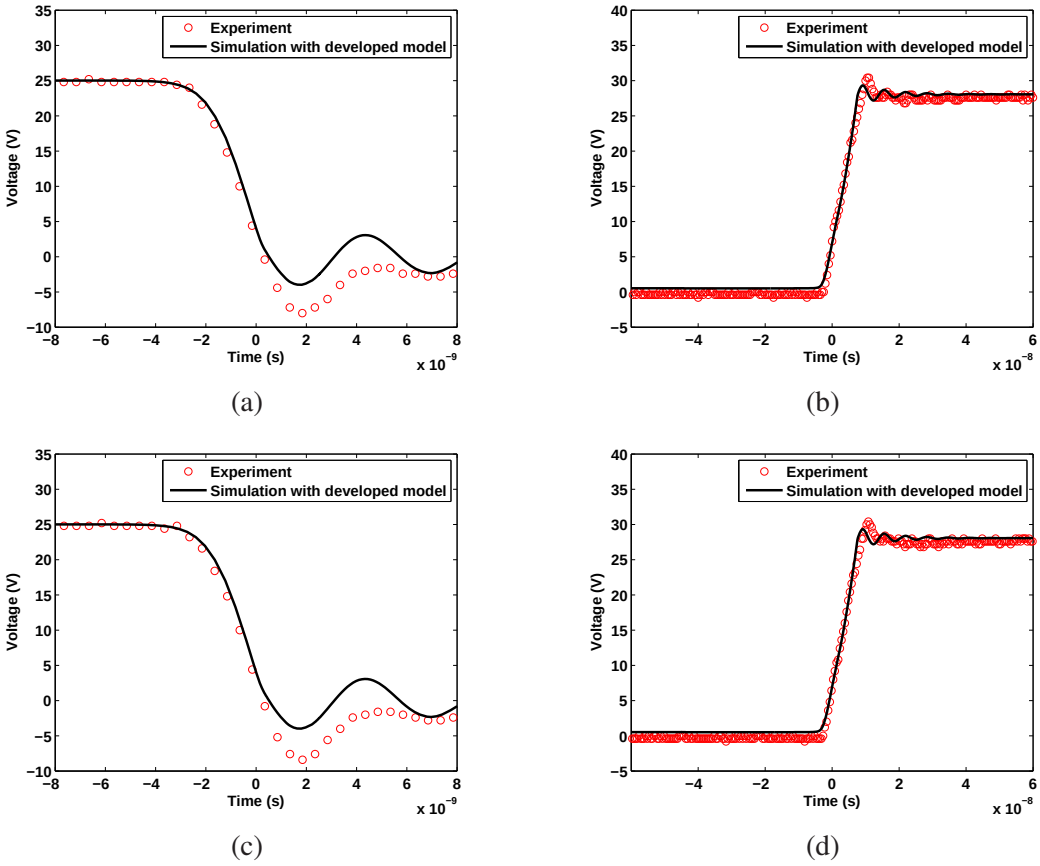
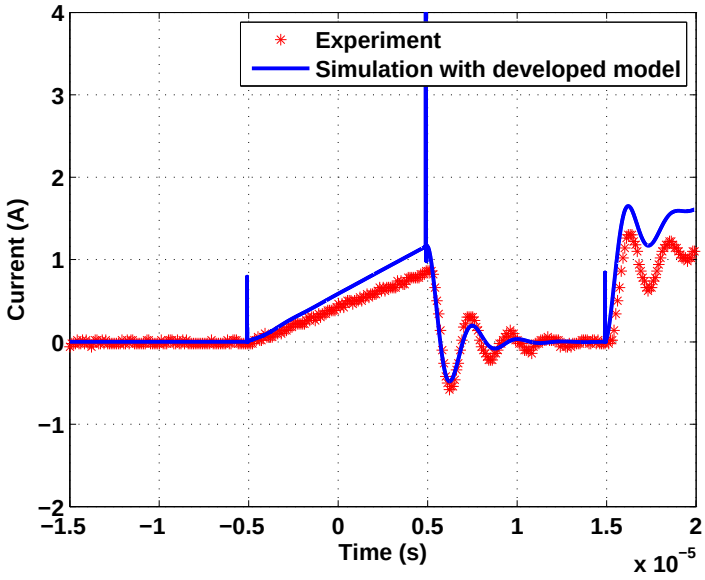


Figure 4.12: Comparison of experimental and simulation results of V_{ds} of the lower switch with parasitics in circuit considered at 50 ^{o}C during (a) and (b) lower switch turn-on and turn-off transients, respectively, and at 70 ^{o}C during (c) and (d) lower switch turn-on and turn-off transients.

system is simulated in the PLECS environment with its steady state analysis tool as in Fig. 4.15(b). Since the IR thermal imager measures the case temperature of the device, for a meaningful comparison, case temperature estimations are obtained by subtracting the junction-case temperature drop calculated by the junction-case thermal network provided in [63] from the junction temperature estimation obtained directly from the simulations. The case temperature of the GaN FET (lower switch) increases from 34.3 ^{o}C to 44.3 ^{o}C during 5 minutes of operation, while the estimated final temperature, based on the developed and PLECS models, is 44.94 ^{o}C and 44.96 ^{o}C, respectively. As shown in Fig. 4.15, the final case temperature of device as well as the trend of temperature increase obtained from the developed model is very close to that from thermal measurement.



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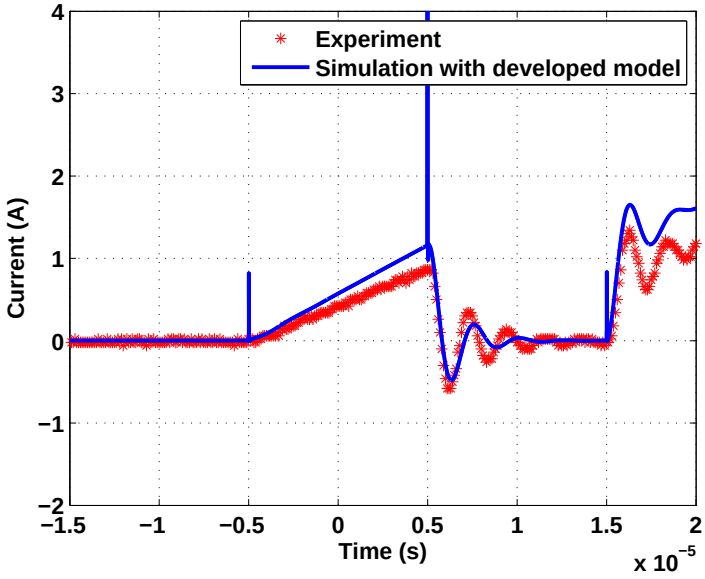
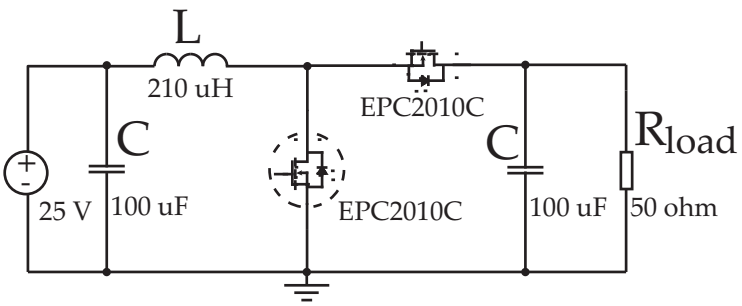


(b)

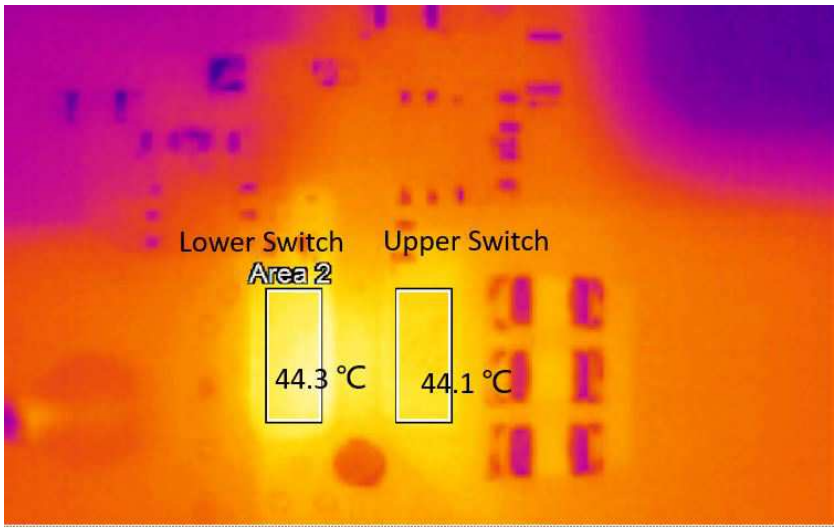
Figure 4.13: Comparison of experimental and simulation results of current through the lower switch with parasitics in circuit considered at (a) 50 ^{o}C and (b) 70 ^{o}C respectively.

4.4 Conclusions

A new behavioral electro-thermal model for GaN FETs that considers the self-heating and thermal effects on the device characteristics is developed. The model, which is developed



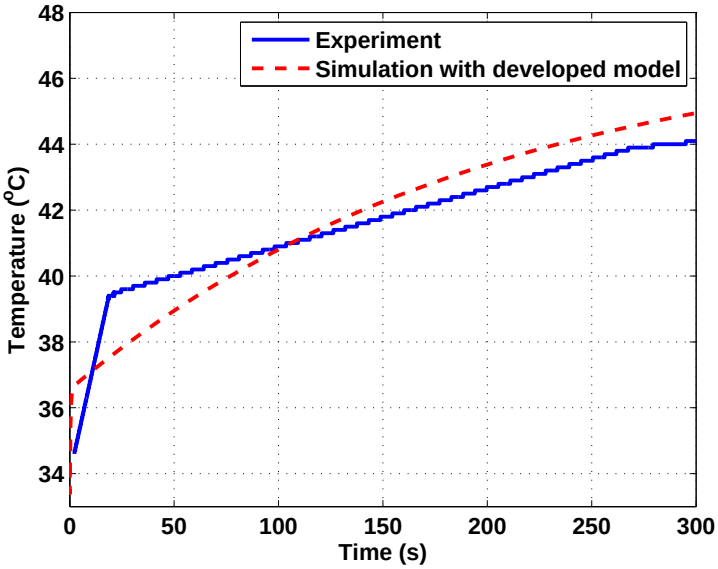
(a)



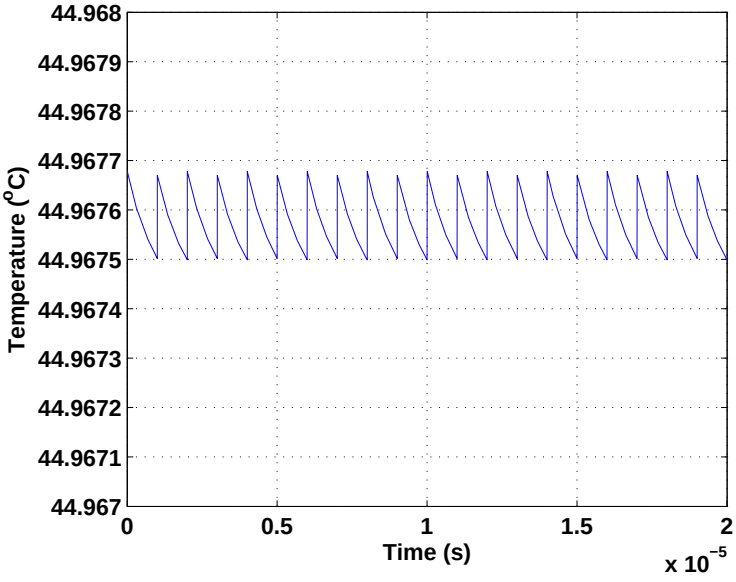
(b)

Figure 4.14: (a) Boost converter setup and (b) thermal image of the boost converter focusing on GaN FETS operating in steady state.

in the LTSPICE software environment, is validated under both conduction and switching conditions and is compared against an available electrical model. To demonstrate the capability/accuracy of the developed model in estimating the junction temperature transients, simulation studies are conducted on a boost converter benchmark system. Experiments are also carried out to validate the developed model. The switching performance results from the proposed model is closely matched with the experimental results obtained from a DPT circuit at different temperatures. The case temperature estimation based on the developed model is also closely aligned with thermal measurement of the GaN FET during its operation in a boost converter system and with the simulation results from PLECS. The developed electro-thermal model for GaN FET is capable of accurately modeling the tem-



(a)



(b)

Figure 4.15: Case temperature of the GaN FET (a) based on the developed model in the LT-SPICE and experimental measurement during 5 minutes of operation in the boost converter system and (b) based on PLECS steady state analysis.

perature impacts on device characteristics as well as estimating the device temperature in the SPICE circuit simulations.

CHAPTER 5
MODELING AND CONTROL OF THE MODULAR MULTILEVEL CLAMPED CAPACITOR CONVERTER (MMC3)

5.1 Fundamental Model of Switched Capacitor (SC) Converter

Any SC converter can be represented by an ideal two-port equivalent circuit presentation as shown in Fig. 5.1(a), where V_{in} is the input voltage, n represents the voltage gain of the converter, R_o is the equivalent output impedance and R_L represents the load [66]. This is referred to as the fundamental model of SC converters. Since SC converters are based on networks of capacitors and resistors, the output impedance is a function of switching frequency. When the switching frequency is relatively low, the impedances of capacitors dominate the output impedance. Thus, the output impedance is inversely-propotional to the switching frequency. This case is referred to as the Slow Switching Limit (SSL). In this case, the capacitor voltages reach steady-state before each switching transition and the capacitor currents are in the form of discontinuous pulses. On the other hand, as switching frequency becomes higher, the impedances of the capacitors become smaller and the on-state resistance of power devices and equivalent series resistance (ESR) of capacitors dominate the output impedance. This is referred to as the Fast Switching Limit (FSL) and the output impedance is thus independant of switching frequency. In this case, the capacitor voltages do not reach steady-state before the next switching transition and capacitor currents are continuous [66]. The overall relationship of output impedance and switching frequency can thus be depicted as in Fig. 5.1(b). Based on this fundamental model, the output voltage of any SC converter can be expressed as

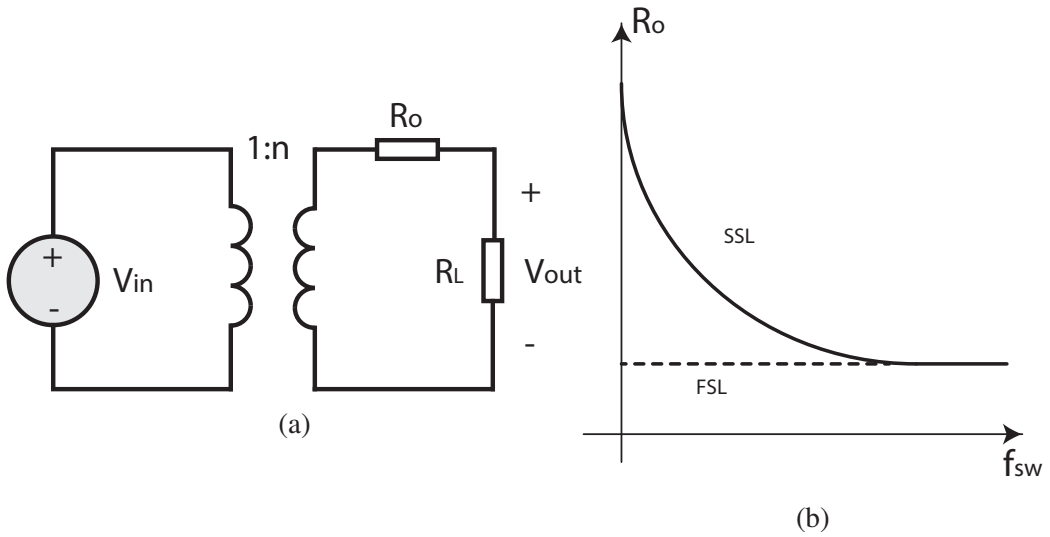


Figure 5.1: (a) Fundamental model of an SC converter and (b) output impedance vs. frequency for SSL and FSL cases.

$$V_o = nV_{in} - I_o R_o = nV_{in}\frac{R_L}{R_L + R_o}, \tag{5.1}$$

where $I_o = \frac{V_{out}}{R_L}$ is the load current.

As shown in equation (5.1), to maximize the voltage conversion ratio, i.e., system efficiency, the output impedance should be as low as possible. On the other hand, the conversion ratio can be modified by modulating the output impedance. However, the output impedance can be varied by changing switching frequency only when system is in the SSL region, and will remain constant after system enters the FSL region. Thus, the converter should be designed to work in the SSL region for output regulation capability, but close to the intersection frequency of SSL and FSL region for high efficiency.

In the following sections, first, a detailed time-domain model of the MMC3 in boost mode of operation is developed to enable accurate calculation of output voltage as well as capacitor voltages and currents, which is matched with the fundamental model of SC converters. Then, a closed-loop voltage control strategy is proposed for the MMC3 based on Pulse Dropping Technique (PDT) and insertion/bypass of SubModules (SMs). State-

space small-signal models are derived for the converter to analyze the stability of both open-loop and closed-loop systems. At the end of this chapter, simulation results are provided to validate the proposed control strategy. Experimental results and validation are shown in Chapter 7. The analysis, model and proposed control strategy in this chapter can be easily extended and applied to the MMC3 in the buck mode of operation.

5.2 Time-domain Model of the MMC3

The circuit diagram of an $(n+1)$-level MMC3 is shown in Fig. 5.2. The MMC3 consists of n identical SMs with each SM comprised of one capacitor, one diode and two power switches. There is an additional diode at the high-voltage side of the converter and a large capacitor at the output. The theoretical output voltage of the MMC3 is equal to $(n+1)V_{low}$. The MMC3, due to its multilevel structure, can conceptually meet any voltage level requirement. Another feature of the MMC3 is its low complexity in control. The two switches in each SM are controlled in a complementary manner, constituting only two switching states. The two switching states of a 5-level MMC3 are shown in Fig. 5.3 as an example. During state (a), all switches in black color conduct while those in grey block, and capacitors C_1 and C_3 get charged while C_2 and C_4 get discharged. During state (b), the opposite happens and C_2 and C_4 charge while C_1 and C_3 discharge. During steady-state operation with open-loop control, each of the two states lasts for a duration of $T/2$, where T is the switching period. Based on the two switching states, the maximum voltage of the capacitor C_n in Fig. 5.2 is nV_{lv} while the maximum blocking voltage is only V_{lv} for the switches and $2V_{lv}$ for the diodes. In addition, by considering redundant SMs in the system, any failed SM can be bypassed while the converter continues its normal operation in a seamless manner, which can enhance system reliability [6].

In order to understand the operation principle and performance of the MMC3 system, a detailed time-domain model is derived to express the output voltage, capacitor voltage ripples and current between the SMs as functions of load current, switching frequency and

SM/output capacitances. Without loss of generality, a 5-level MMC3 system is used as an example.

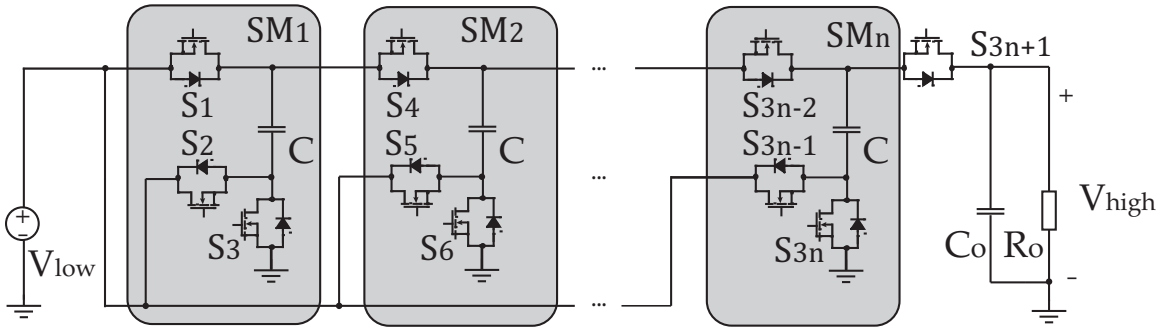


Figure 5.2: Circuit diagrams of an $(n+1)$-level MMC3.

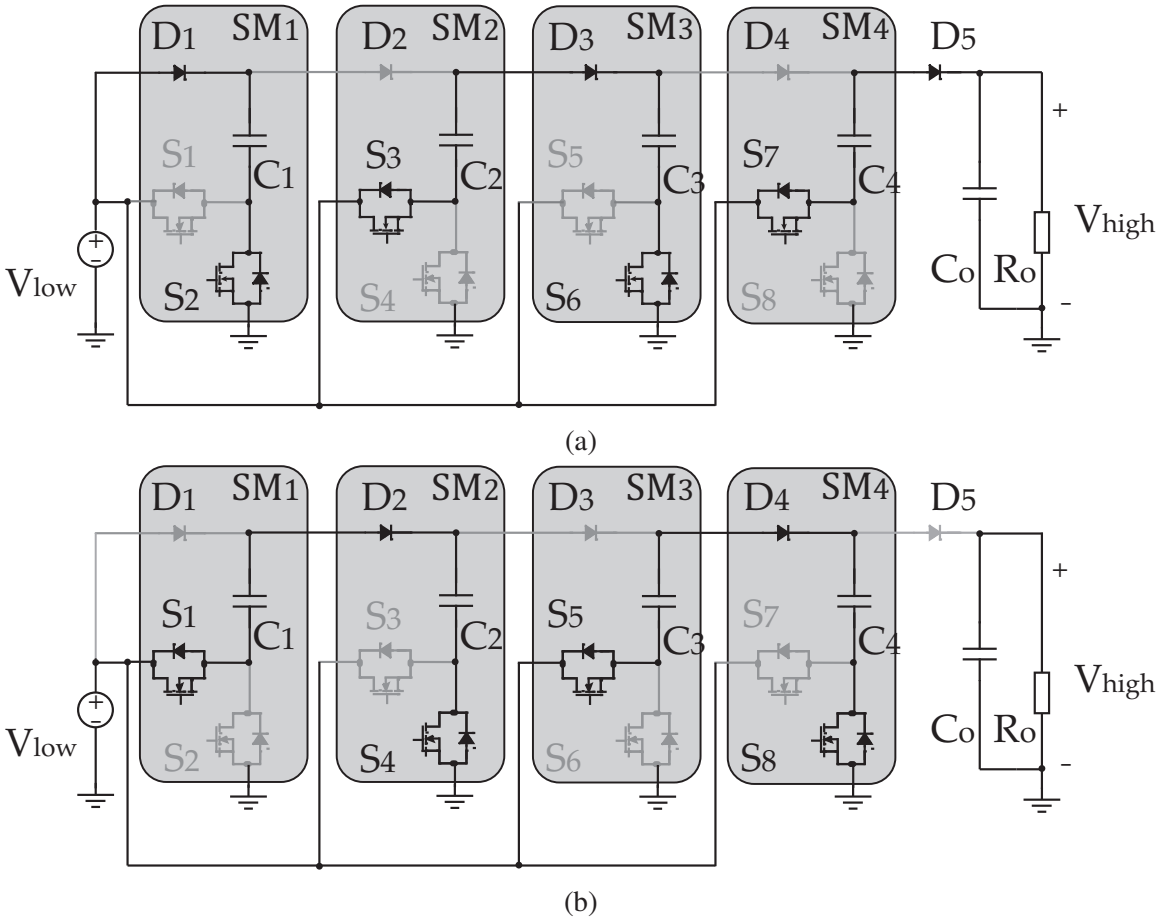


Figure 5.3: Two switching states of a 5-level MMC3.

To derive the time-domain model of MMC3 during steady-state operation under open-

loop control, a set of assumptions are made as follows:

- the converter has a DC output voltage with very small ripple due to its very high switching frequency.
- the SM capacitors have reached steady state prior to each switching state transition due to very small time constant.
- the net change of each capacitor voltage over one switching period is zero, i.e., $V_c(t+T) = V_c(t)$.
- the output stage has a much larger time constant compared with that of a SM.

5.2.1 Output Voltage Ripple

Derivation of the time-domain model starts by determining the output voltage ripple accurately. The output stage of the converter during its two switching states is shown in Fig. 5.4. During the state shown in Fig. 5.4(a), the output capacitor C_o gets charged with i_4 and discharged by the load current I_R. During the state shown in Fig. 5.4(b), C_o is discharged only by the load current. Thus, with the third assumption, i.e., capacitor charge balance, the following relationship holds for C_o:

$$\int_t^{t+\frac{T}{2}} i_4 dt - \int_t^{t+\frac{T}{2}} I_R dt = \int_{t+\frac{T}{2}}^{t+T} I_R dt. \tag{5.2}$$

Based on (5.2) and the first assumption, we have

$$\int_t^{t+\frac{T}{2}} i_4 dt = \int_t^{t+T} I_R dt = I_R T = \frac{V_o}{R_o f}, \tag{5.3}$$

where V_o is the output voltage and f is the switching frequency. Considering the fourth assumption, the output voltage ripple is determined by the charge from i_4:

$$\Delta V_o = \frac{\int_t^{t+\frac{T}{2}} i_4 dt - \int_t^{t+\frac{T}{2}} I_R dt}{C_o} = \frac{V_o}{2R_o C_o f}. \tag{5.4}$$

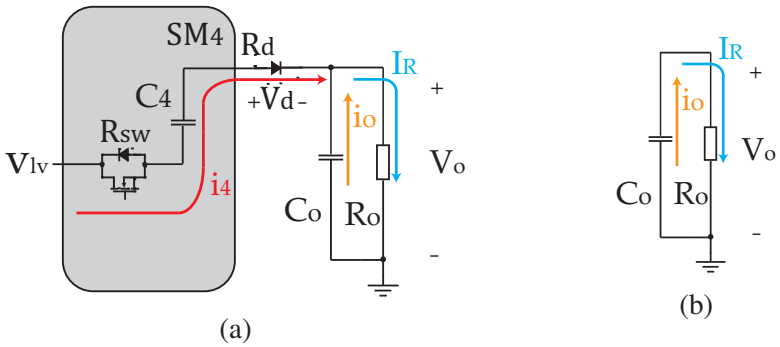


Figure 5.4: Output stage of a 5-level MMC3 during boost operation with (a) odd-numbered on-state switches and (b) even-numbered on-state switches.

5.2.2 SM Capacitor Voltage Ripple

Based on (5.3), the voltage ripple of C_4 is:

$$\Delta V_4 = \frac{\int_t^{t+\frac{T}{2}} i_4 dt}{C_4} = \frac{V_o}{R_o C_4 f}. \tag{5.5}$$

During the switching state shown in Fig. 5.3(b), capacitor C_3 charges C_4. As the capacitances are equal and they are in series, the voltage decrease of C_3 is equal to the voltage increase of C_4, i.e., ΔV_3=ΔV_4. With the same procedure, it can be proved that all SM capacitors have the same voltage ripple magnitude. Thus, we have,

$$\Delta V_{SM} = \frac{V_o}{R_o C_{SM} f}, \tag{5.6}$$

where ΔV_{SM} is the voltage ripple magnitude of each SM capacitor and C_{SM} is the capacitance of SM capacitors.

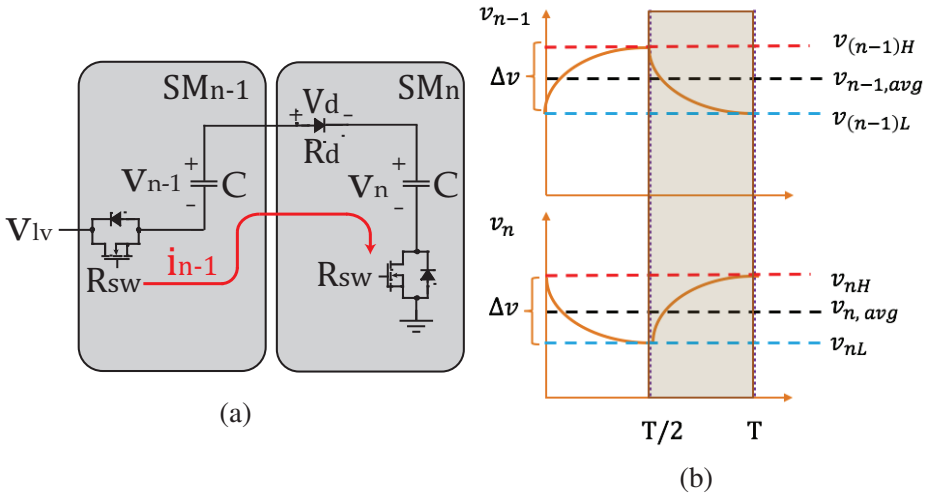


Figure 5.5: (a) Typical connection diagram between two SMs and (b) their capacitor voltage waveforms.

5.2.3 Average Output Voltage

Based on the mathematical derivations for capacitor voltage ripples from Subsections 5.2.1 and 5.2.2, the average output voltage of the MMC3 can be calculated. A typical way of connection between two SMs in conjunction with the SM capacitor voltages of the MMC3 over one switching cycle are shown in Figs. 5.5(a) and (b), respectively. In Fig. 5.5, V_{lv} is the supply voltage, V_d is the diode forward voltage drop, v_{nH}, $v_{n,avg}$ and v_{nL} represent the highest, average and lowest voltages of capacitor C_n, respectively, and $v_{(n-1))H}$, $v_{n-1,avg}$ and $v_{(n-1)L}$ represent the voltages of capacitor $C_{(n-1)}$. In the following analysis, it is assumed that the two SMs become connected after $t = T/2$. At the end of the switching cycle, the circuit has reached steady state and we have:

$$v_{nH} = V_{lv} + v_{(n-1)L} - V_d. \tag{5.7}$$

Based on Fig. 5.5(b),

$$v_{nH} = v_{n,avg} + \frac{\Delta V_{SM}}{2} \tag{5.8}$$

and

$$v_{(n-1)L} = v_{(n-1),avg} - \frac{\Delta V_{SM}}{2}. \tag{5.9}$$

Based on (5.7), (5.8) and (5.9), the average voltage of C_n is derived as

$$v_{n,avg} = V_{lv} + v_{(n-1),avg} - V_d - \Delta V_{SM}. \tag{5.10}$$

Following a similar procedure, the average capacitor voltage of the first SM and the average output voltage of the converter can be expressed by

$$v_{1,avg} = V_{lv} - V_d - \frac{\Delta V_{SM}}{2}, \tag{5.11}$$

and

$$V_o = (n+1)V_{lv} - (n+1)V_d - n\Delta V_{SM} - \frac{\Delta V_o}{2}. \tag{5.12}$$

Subsitituting equations (5.4) and (5.6) into (5.12), we have

$$\begin{aligned} V_o &= (n+1)V_{lv} - I_o R_o, \\ R_o &= \frac{n}{fC_{SM}} + \frac{1}{2fC_o}, \end{aligned} \tag{5.13}$$

which is in the same form as in equation (5.1) derived from the fundamental model of SC converters. In [66], the output impedance of an SC converter operating in SSL is derived as

$$R_o = \sum_{i=1}^{n+1} \sum_{j=1}^{k} \frac{(a_i^j)^2}{2C_i f}, \tag{5.14}$$

where C_i is the capacitance of the ith capacitor in system, and a_i^j is the charge flowing into the i'th capacitor during the jth switching state normalized to the total output charge in a complete switching period. In the MMC3, based on the previous analysis, k is equal to 2 as only two switching states are available and n is equal to the number of SMs. For any SM capacitor in the system, $a_i^j = 1$ is valid due to the charge balance discussed in Sections 5.2.1 and 5.2.2. For the output capacitor, $a_{n+1}^1 = 1$ and $a_{n+1}^2 = 0$ according to [66]. With these judgements, it is clear the equations (5.13) and (5.14) are equivalent, and the derived time-domain model agrees with the fundamental model of SC converters.

5.2.4 Stress of Components

During the design process of the MMC3, for proper component sizing, it is important to determine the voltage/current stresses of the components, i.e., switches and capacitors. Based on the derivations in previous sections and Fig. 5.2, the maximum voltage of the capacitor C_n is nV_{lv}, and the maximum blocking voltage of the switches is V_{lv} for switches $S_{(3n+2)}$, $S_{(3n+3)}, n = 0, ..., 3$, and $S_{(3n+1)}, n = 0, 4$, and $2V_{lv}$ for switches $S_{(3n+1)}, n = 1, ..., 3$.

To determine the peak and RMS current stresses of the components, the maximum voltage mismatch between two capacitors of the connected SMs needs to be calculated. Based on Fig. 5.5(b), the the maximum mismatch between capacitor voltages occur at the point of switching transition and is equal to $2\Delta V_{SM}$. The peak current between the connected SMs is then derived as

$$I_{peak} = \frac{2\Delta V_{SM}}{2R_{sw} + R_d}, \tag{5.15}$$

where R_{sw} and R_d are on-state resistances of the switch and diode (or switch in reverse-conduction), respectively. Similarly, the peak currents into the first SM and last SM are derived as

$$I_{peak,first} = \frac{\Delta V_{SM}}{R_{sw} + R_d}, \text{and} \tag{5.16}$$

$$I_{peak,last} = \frac{(\Delta V_{SM} + \Delta V_o)}{R_{sw} + R_d}. \tag{5.17}$$

Based on the circuit analysis in Fig. 5.5(a) with Laplacian Transform, the instant current through the power devices at time t is calculated to be

$$i(t) = I_p e^{-\lambda t}, \tag{5.18}$$

and the RMS current is given by

$$I = I_p \sqrt{\frac{1 - e^{-\lambda T}}{2\lambda T}}, \tag{5.19}$$

where I_p is the peak current value from (5.15), (5.16) or (5.17) depending on the case and $\lambda = \frac{2}{(2R_{sw}+R_d)C_{SM}}$ for the connected SMs in the middle, $\lambda = \frac{2}{(R_{sw}+R_d)C_{SM}}$ for the first SM and $\lambda = \frac{C_{SM}+C_o}{(R_{sw}+R_d)C_{SM}C_o}$ for the last SM.

5.2.5 Effect of Parasitic Inductance

In power converters, the PCB traces and equivalent series inductance of components, e.g., capacitors and power devices, induce parasitic inductances into the system. In this section, the effect of the parasitic inductances on converter design is revealed, and the switching

frequency of the converter is determined to achieve Zero-Current Switching (ZCS) for the power devices.

Impact on output voltage

To obtain accurate values of the output voltage and capacitor current of the MMC3, the parasitic inductances existing in the current loops must be taken into account. In the MMC3, the parasitic inductance in the current loop between two SMs can be modeled as one single inductance, as shown in Fig. 5.6. The current loop can be simplified into an equivalent RLC series resonant circuit as in Fig. 5.8(a). If the R, L and C in the circuit satisfy the relationship as in equation (5.20), the system will feature an underdamped response, which allows the inductor current to cross zero in half the resonant period. In that case, the current in the circuit is a sinusoidal waveform with exponentially decreasing amplitude. In a Dickson converter, due to the presence of the diode, the current will not become negative after its zero crossing, but stay at zero until the next cycle, as shown in Fig. 5.8(b). For the MMC3, however, this has to be achieved by accurate timing of control signals.

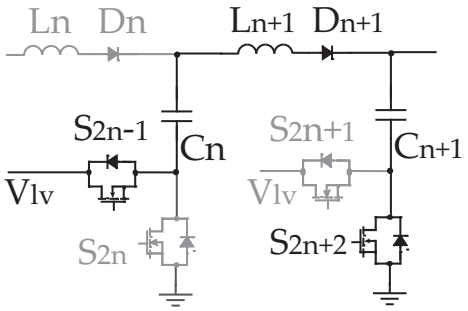


Figure 5.6: Parasitic inductance between SMs of the MMC3.

$$\frac{R}{2}\sqrt{\frac{C}{L}} < 1 \tag{5.20}$$

The SM capacitor voltage and current waveforms without and with the impacts of parasitic inductance are shown in Fig. 5.7(a) and (b), respectively. In both figures, during the first half switching period, the capacitor gets charged by an input voltage of V_{in}, and it

is discharged during the second half period. In Fig. 5.7(a), the capacitor voltage reaches steady-state after charging, achieving a maximum value of V_{in}. Thus, the average voltage of the capacitor is below V_{in} even when an ideal charging path with no lossy component is assumed. This is also the physical meaning of the output impedance of SC converters. However, when the parasitic inductance is present, the charging process will continue even when the capacitor voltage is higher than V_{in}. In that case, when the switching frequency is no more than the LC resonant frequency as shown in Fig 5.7(b), and lossy components in the circuit are ignored, the average voltage of the capacitor can reach V_{in}. In this sense, the parasitic inductance in the circuit helps to increase the SM capacitor and total output voltage of the MMC3. In the case as in Fig 5.7(b), the output voltage of the system should no longer be calculated using equation (5.12). Instead, the output voltage is mainly affected by diode forward voltage drop and lossy components in the current path, and thus can be expressed by

$$V_o = (n+1)V_{lv} - (n+1)V_d - I_o R_{loss} - \frac{\Delta V_o}{2}, \tag{5.21}$$

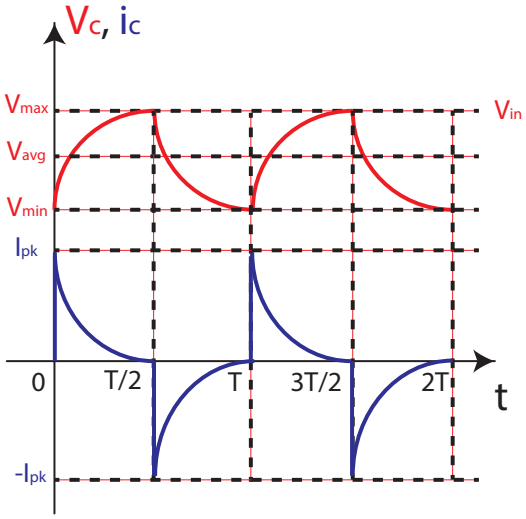
$$R_{loss} = (n+1)R_d + 2nR_{sw} + 2(n+1)R_C, \tag{5.22}$$

where R_d, R_{sw} and R_C are the resistance of the diode, the power switch and the equivalent series resistance of the capacitor, respectively.

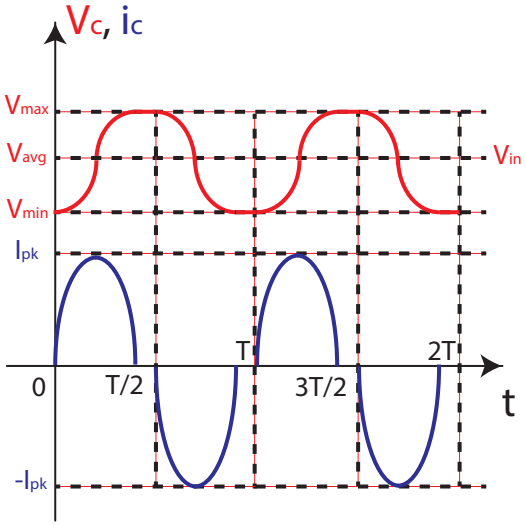
Impact on capacitor current

Parasitic inductance also impacts the shape and value of capacitor current as shown in Fig. 5.7. When ignoring the parasitic inductance, the peak and RMS values of current are calculated in Section 5.2.4. When parasitic inductance is considered, the mathematical expressions of the current between the connected SMs can be derived as

$$i_{SM} = \frac{2\Delta V_{SM} - V_d}{L_{SM} w_d} e^{-\alpha t} \sin(w_d t), \tag{5.23}$$



(a)



(b)

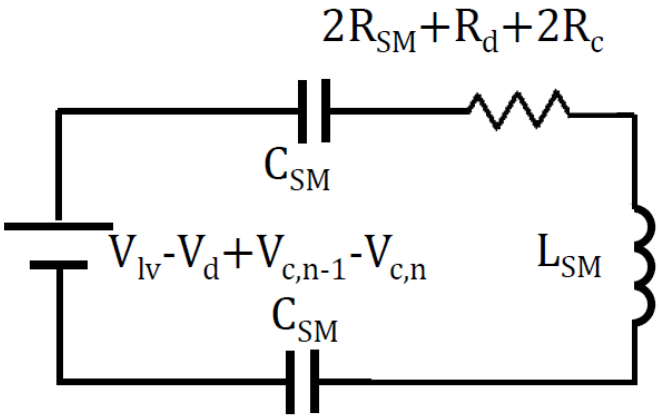
Figure 5.7: SM capacitor voltage and current waveforms (a) without considering parasitic inductance and (b) considering parasitic inductance with underdamped inductor current.

where

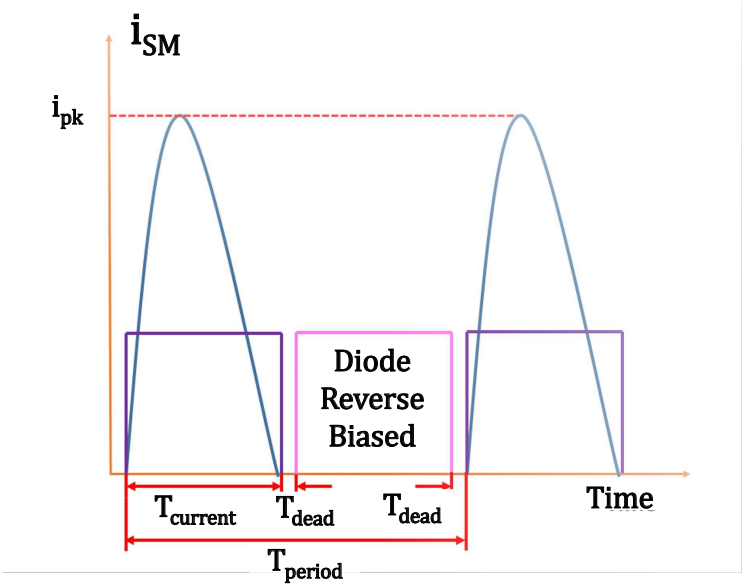
$$w_d = \sqrt{\frac{2}{L_{SM}C_{SM}} - \frac{R^2}{4L_{SM}^2}}, \tag{5.24}$$

$$\alpha = \frac{R}{L_{SM}}, \tag{5.25}$$

$$R = 2R_{sw} + 2R_c + R_d, \tag{5.26}$$



(a)



(b)

Figure 5.8: (a) Simplified circuit diagram of two SMs and (b) shape of underdamped SM current.

and R_{sw}, R_d and R_c are on-state resistances of the switch, the diode, and the equivalent series resistance of the SM capacitors, respectively. Assuming that the current is the positive half of a pure sinusoidal waveform with an exponential decay in magnitude, the peak current occurs at $t = T_{SM}/4$, where T_{SM} is the period of the sinusoidal waveform, and the peak and RMS values of current can be derived as

$$I_{SM,peak} = \frac{2\Delta V_{SM} - V_d}{L_{SM} w_d} e^{-\alpha \frac{T_{SM}}{4}}, \text{ and} \tag{5.27}$$

$$I_{SM} = \sqrt{\frac{\int_0^{T_{SM}/2} i_{SM}^2 dt}{T_{SM}}} = \frac{I_{SM,peak}}{2}. \tag{5.28}$$

Achieving ZCS

Another important information here is that if the R, L and C in the circuit satisfy the relationship as in equation (5.20), the system will feature an underdamped response, which allows the inductor current to cross zero in half the resonant period, i.e, $T_{SM}/2$. In this case, by designing the on-time of each switch in one switching period, $T_{current}$, equal to or larger than $T_{SM}/2$, the current through all power devices will be zero at turnoff as shown in Fig. 5.8(b). As the inductor current will always build up from zero after turning the power devices on, ZCS turn-on is always guaranteed. Thus, full ZCS operation can be achieved for the MMC3 when

$$T_{current} = (T_{period} - 2T_{dead})/2 = T_{SM}/2. \tag{5.29}$$

It should be pointed out that the power switches S_2 and S_{2n-1} as in Fig. 5.2 will require a longer on-time to achieve ZCS because their current loop is only consisted of one SM capacitor and the resulting w_d is smaller. However, it is desirable to achieve full ZCS operation for all other switches while maintaining a reasonable switching frequency to reduce output voltage ripple and conduction loss. Thus, the switching frequency can be determined based on equation (5.29).

5.3 The Proposed Closed-loop Control of the MMC3

The output voltage of the MMC3 can be modulated by using the PDT [67]. Lately, the PDT is proposed as a basis for closed-loop voltage control of the MMC3 [68]. In this

section, first, the PDT is described and analyzed in detail, and a feedback control strategy is proposed for the MMC3, which bases upon both the PDT and the insertion/bypass of SMs to regulate the output voltage.

5.3.1 The PDT

The PDT generates the gating signals of the switches by comparing a square wave with an adjustable amplitude with a fixed-amplitude triangular wave [67], as shown in Fig. 5.9. Similar to the conventional Pulse-Width Modulation (PWM) technique, amplitude and frequency modulation indices m_a and m_f are defined as the ratio between amplitude and frequency of the square wave vs. those of triangular wave, respectively. When the instantaneous value of the square wave is larger than the triangular wave, the output is high, and vice versa. m_a is in the range of zero to one. Thus, when m_a is equal to one, the gate signals will be the same as the square wave, and when m_a becomes smaller than one, pulses will be dropped in the gate signals, as shown in Fig. 5.9. It has been shown in [67] that m_a has a significant impact on the CR of the MMC3, while m_f mainly affects the range of variation in CR. Thus, by setting an appropriate m_f and varying m_a, the CR of the MMC3 can be varied within a range, instead of being fixed by the SM number. For example, with $m_f = 10$, it is possible to obtain a CR between 3.9 to 4.8 with a 4-SM MMC3 for boost operation by varying m_a from 0.2 to 1 [67].

In order to further understand and evaluate the performance of the PDT, it is desired to update the time-domain model derived in Section 5.2 and include the impact of the PDT. Figure. 5.10 shows the output voltage waveform and the capacitor voltage of the last SM when $m_a = 0.5$. The output voltage ripple can be expressed by

$$\Delta V_o = \frac{I_R(1 - m_a)T_{PDT}}{C_o}. \tag{5.30}$$

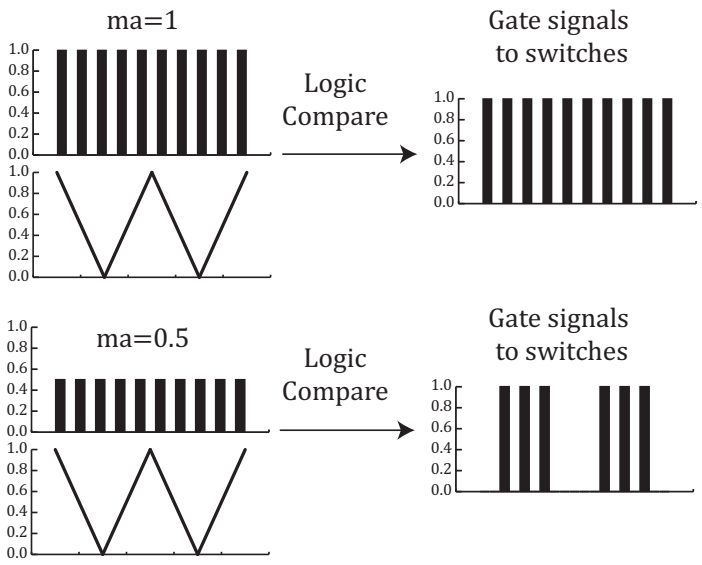


Figure 5.9: Gate signals generated with different m_a values using the PDT method.

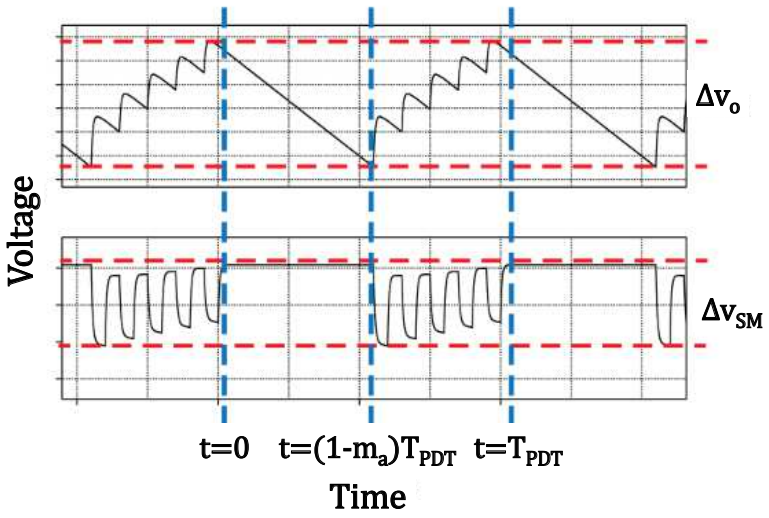


Figure 5.10: Output voltage waveform (upper) and voltage of SM_n (lower) with $m_a = 0.5$ applied.

In steady state, as proved in Section 5.2.2, all SM capacitors have the same peak-to-peak voltage ripple. Based on capacitor charge balance, the ripple component of the SM capacitor voltage can be derived as

$$C_{SM}\frac{m_a T_{PDT}}{T}\Delta V_{SM} = I_R T_{PDT}, \tag{5.31}$$

$$\Delta V_{SM} = \frac{I_R T}{C_{SM} m_a} = \frac{V_o}{R_o C_{SM} m_a f}. \tag{5.32}$$

It can be seen that the voltage ripple of SM capacitors under the PDT is $\frac{1}{m_a}$ times larger than that in the original system as shown in equation (5.6). Thus, based on (5.12), under the PDT, the average output voltage of the converter is

$$V_o = (n+1)V_{lv} - (n+1)V_d - \frac{nI_R T}{C_{SM} m_a} - \frac{I_R(1-m_a)T_{PDT}}{4C_o}. \tag{5.33}$$

Based on (5.33), as m_a decreases, the output voltage will decrease due to the increase of the last two terms, i.e., the SM capacitor and output voltage ripple, respectively. In addition, the contribution of the SM capacitor voltage ripple to the output voltage modulation is much more significant than that of the output voltage ripple due to presence of n in the nominator and m_a in the denominator. In conclusion, the PDT can achieve an adjustable CR by adjusting the SM capacitor voltage ripple.

5.3.2 Insertion/Bypass of SMs

As the MMC3 is comprised of several identical SMs, additional redundant SMs can be considered such that they are normally bypassed and can be inserted when a SM fails, i.e., cold reserve SMs. The SMs in the MMC3 can also be bypassed/inserted as a means to increase the range of output voltage, as the output voltage is a function of the number of SMs. To bypass a SM (denoted by number k), the switches S_{2k-1} and S_{2k} are kept off regardless of the PWM signals. The gate signals of the switches will be resumed when an insertion command is activated. When the k'th SM is inserted with an initial capacitor

voltage of zero, the charging current will be determined by $V_{k,avg}$ as in equation (5.10). The experimental waveforms of the insertion/bypass of SM during the operation of MMC3 will be shown in Chapter 7. It is thus desired to keep the redundant SMs at the low-voltage side of the converter in order to limit the charging current. Although the insertion/bypass of SMs can also control the output voltage, soft switching is not guaranteed, and significant charging current may occur during the transient. Thus, the insertion/bypass of SMs will be only used in a slow control loop or with manual input.

5.3.3 The Proposed PDT-based Feedback Control

A closed-loop output voltage regulation strategy for the MMC3 is developed based on the PDT and the SM insertion/bypass operation. The proposed control strategy, as demonstrated in Fig. 5.11, consists of an inner (fast) regulation loop and an outer loop. In the inner loop, first, the output voltage of the converter is measured and compared with the reference value. The difference then goes through a PI controller and generates m_a for the PDT-based control. The gate signals for switches are obtained through a PWM between the high-frequency square wave with an amplitude of m_a and the low-frequency triangular waveform with an amplitude of one. In the outer loop, the difference between the reference and output voltage and the m_a index are monitored. If the output voltage is below the reference value and the m_a index is one, the number of SMs in the system should be increased to extend the output voltage range. A time delay, T_{delay}, is applied before delivery of the insertion command to avoid frequent insertion/bypass operations caused by system transients and noise. If the output voltage is higher than the reference value and m_a index is at its minimum allowed level, e.g., 0.1, an SM should be bypassed to reduce the output voltage and to avoid power losses due to a very low m_a index. A time delay is also applied in this case. By combining the inner and outer regulation loops, the output voltage is regulated and the controllable output range is increased.

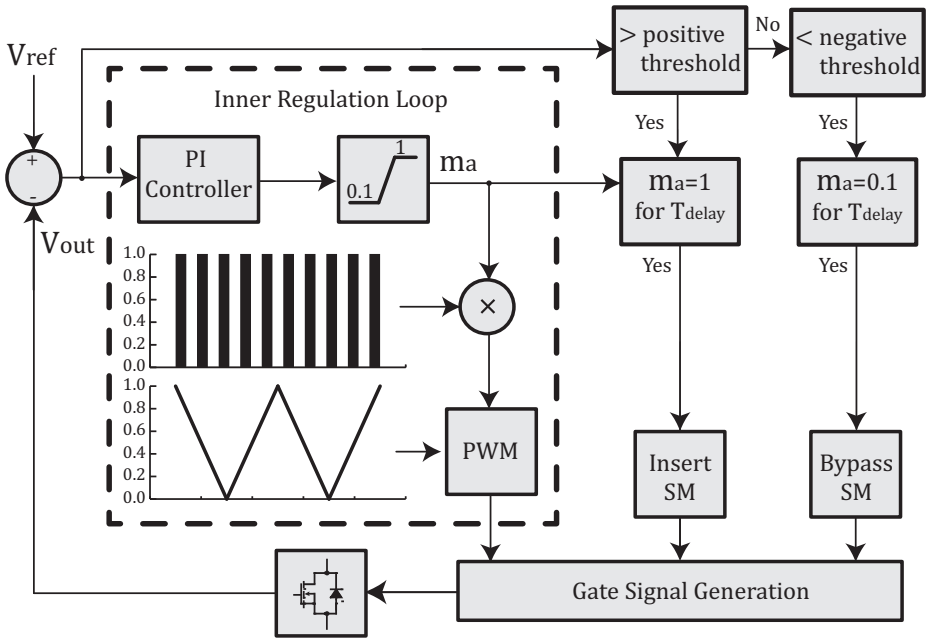


Figure 5.11: The proposed feedback control based on the PDT and SM insertion/bypass operation.

5.4 State-Spcce Small Signal Model of the MMC3

To evaluate the performance of the proposed control strategy, a small-signal state-space model of the converter is derived and the transfer functions of both the open-loop converter and the closed-loop converter with the proposed control strategy are derived. Without loss of generality, a 4-SM MMC3 is analyzed here as an example. The results obtained from this section can be easily extended to the converter with any number of SMs. Besides, only the fast inner loop is considered in this model, as the change in SM number will not affect the stability of the control strategy and have very straightforward effect on the output voltage. In the state-space model, the voltage of each capacitor in the system is considered as a state variable. Input voltage and load current are considered inputs to the system while the output voltage is considered as an output. The existence of parasitic inductance in the system mainly leads to increased capacitor and output voltage values but does not affect the overall stability of the system. Thus, the impact of parasitic inductance is not included in the analysis for simplicity.

5.4.1 Transfer Function of the Open-loop System

In the open-loop converter, based on the switching state shown in Fig. 5.3(a), we have

$$\begin{cases} C\frac{dv_{c1}}{dt} = -\frac{v_{lv}-V_d-v_{c1}}{R_{sw}+R_d+R_c}, \\ C\frac{dv_{c2}}{dt} = -\frac{v_{lv}-V_d+v_{c2}-v_{c3}}{2R_{sw}+R_d+2R_c}, \\ C\frac{dv_{c3}}{dt} = \frac{v_{lv}-V_d+v_{c2}-v_{c3}}{2R_{sw}+R_d+2R_c}, \\ C\frac{dv_{c4}}{dt} = -\frac{v_{lv}-V_d+v_{c4}-v_{co}}{R_{sw}+R_d+2R_c}, \\ C_o\frac{dv_{co}}{dt} = \frac{v_{lv}-V_d+v_{c4}-v_{co}}{R_{sw}+R_d+2R_c} - i_{load}. \end{cases} \tag{5.34}$$

Based on the analysis in Section 5.2, let $x = [v_{c1}; v_{c2}; v_{c3}; v_{c4}; v_{co}]$, $u = [v_{lv}-V_d; -i_{load}]$ and $y = v_{co} - (\frac{4}{Cf} + \frac{1}{4C_of})i_{load}$. Therefore, (5.34) can be rewritten as

$$\begin{cases} \dot{x} = A_1x + B_1u \\ y = C_1x + D_1u, \end{cases} \tag{5.35}$$

where A_1, B_1, C_1 and D_1 are shown in (5.38).

Similarly, for the switching state shown in Fig. 5.3(b), we have

$$\begin{cases} C\frac{dv_{c1}}{dt} = -\frac{v_{lv}-V_d+v_{c1}-v_{c2}}{2R_{sw}+R_d+2R_c}, \\ C\frac{dv_{c2}}{dt} = \frac{v_{lv}-V_d+v_{c1}-v_{c2}}{2R_{sw}+R_d+2R_c}, \\ C\frac{dv_{c3}}{dt} = -\frac{v_{lv}-V_d+v_{c3}-v_{c4}}{2R_{sw}+R_d+2R_c}, \\ C\frac{dv_{c4}}{dt} = \frac{v_{lv}-V_d+v_{c3}-v_{c4}}{2R_{sw}+R_d+2R_c}, \\ C_o\frac{dv_o}{dt} = -i_{load}. \end{cases} \tag{5.36}$$

With the same set of state variables, inputs and output, (5.36) is rewritten as

$$
\begin{cases}
A_1 = \\
\begin{bmatrix}
-\frac{1}{C(R_{sw}+R_d+R_c)} & 0 & 0 & 0 & 0 \\
0 & -\frac{1}{C(2R_{sw}+R_d+2R_c)} & \frac{1}{C(2R_{sw}+R_d+2R_c)} & 0 & 0 \\
0 & \frac{1}{C(2R_{sw}+R_d+2R_c)} & -\frac{1}{C(2R_{sw}+R_d+2R_c)} & 0 & 0 \\
0 & 0 & 0 & -\frac{1}{C(R_{sw}+R_d+2R_c)} & \frac{1}{C(R_{sw}+R_d+2R_c)} \\
0 & 0 & 0 & \frac{1}{C_o(R_{sw}+R_d+2R_c)} & -\frac{1}{C_o(R_{sw}+R_d+2R_c)}
\end{bmatrix} \\
B_1 = \\
\begin{bmatrix}
\frac{1}{C(R_{sw}+R_d+R_c)} & 0 \\
-\frac{1}{C(2R_{sw}+R_d+2R_c)} & 0 \\
\frac{1}{C(2R_{sw}+R_d+2R_c)} & 0 \\
-\frac{1}{C(R_{sw}+R_d+2R_c)} & 0 \\
\frac{1}{C_o(R_{sw}+R_d+2R_c)} & \frac{1}{C_o}
\end{bmatrix}
\qquad
C_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix}
\qquad
D_1 = \begin{bmatrix} 0 & \frac{4}{Cf} + \frac{1}{4C_of} \end{bmatrix}
\end{cases}
\tag{5.38}
$$

$$
\begin{cases}
A_2 = \\
\begin{bmatrix}
-\frac{1}{C(2R_{sw}+R_d+2R_c)} & \frac{1}{C(2R_{sw}+R_d+2R_c)} & 0 & 0 & 0 \\
\frac{1}{C(2R_{sw}+R_d+2R_c)} & -\frac{1}{C(2R_{sw}+R_d+2R_c)} & 0 & 0 & 0 \\
0 & 0 & -\frac{1}{C(2R_{sw}+R_d+2R_c)} & \frac{1}{C(2R_{sw}+R_d+2R_c)} & 0 \\
0 & 0 & \frac{1}{C(2R_{sw}+R_d+2R_c)} & -\frac{1}{C(2R_{sw}+R_d+2R_c)} & 0 \\
0 & 0 & 0 & 0 & 0
\end{bmatrix} \\
B_2 = \\
\begin{bmatrix}
-\frac{1}{C(2R_{sw}+R_d+2R_c)} & 0 \\
\frac{1}{C(2R_{sw}+R_d+2R_c)} & 0 \\
-\frac{1}{C(2R_{sw}+R_d+2R_c)} & 0 \\
\frac{1}{C(R_{sw}+R_d+2R_c)} & 0 \\
0 & \frac{1}{C_o}
\end{bmatrix}
\qquad
C_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix}
\qquad
D_2 = \begin{bmatrix} 0 & \frac{4}{Cf} + \frac{1}{4C_of} \end{bmatrix}
\end{cases}
\tag{5.39}
$$

$$
\begin{cases}
\dot{x} = A_2 x + B_2 u \\
y = C_2 x + D_2 u,
\end{cases}
\tag{5.37}
$$

where A_2, B_2, C_2 and D_2 are shown in (5.39).

In the open-loop MMC3, each of the two switching states lasts for half switching cycle. Thus, by averaging (5.35) and (5.37) over one switching cycle, we have

$$
\begin{cases}
\dot{x} = \frac{1}{2}(A_1 + A_2)x + \frac{1}{2}(B_1 + B_2)u, \\
y = \frac{1}{2}(C_1 + C_2)x + \frac{1}{2}(D_1 + D_2)u,
\end{cases}
\tag{5.40}
$$

To derive the small-signal model of the system, based on the state-space averaging

method mentioned in [69], we assume

$$\begin{cases} x = X + \hat{x}, \\ y = Y + \hat{y}, \\ u = U + \hat{u}, \end{cases} \tag{5.41}$$

where symbols with capital letters represent the DC values while the symbols with hats represent the small-signal AC values. The small signal model of the converter is then obtained by substituting (5.41) into (5.40):

$$\begin{cases} \dot{\hat{x}} = \frac{1}{2}(A_1 + A_2)\hat{x} + \frac{1}{2}(B_1 + B_2)\hat{u}, \\ \hat{y} = \frac{1}{2}(C_1 + C_2)\hat{x} + \frac{1}{2}(D_1 + D_2)\hat{u}, \end{cases} \tag{5.42}$$

With the state space model in (5.42), the transfer functions of the open-loop MMC3 can be derived. Since the expressions of the transfer functions are parametric, to simplify their forms, numerical transfer functions based on the system parameters specified in Table 5.1 are provided in (5.43).

Table 5.1: System parameters for transfer function derivation

Parameter	Symbol	Value
Switching frequency	f	500 kHz
Input voltage	V_{lv}	4.42 V
SM capacitance	C	2.2 uF
Output capacitance	C_o	10 uF
Switch on-resistance	R_{sw}	20 mΩ
Diode on-resistance	R_d	20 mΩ
Diode forward voltage drop	V_d	0.7 V
Capacitor equivalent series resistance	R_C	10 mΩ
Proportional gain	K_p	0.1
Integral gain	K_i	100

The Bode diagrams of the open-loop system are given in Fig. 5.12. Both $\hat{v}_o(s)/\hat{v}_{lv}(s)$ and $\hat{v}_o(s)/(-\hat{i}_{load}(s))$ demonstrate large gain magnitude at low frequencies, which leads to

$$\begin{cases} \frac{\hat{v}_o(s)}{\hat{v}_{lv}(s)} = \frac{8.33\times10^5(s+1.028\times10^7)(s+8.752\times10^6)(s+3.926\times10^6)(s+1.475\times10^6)}{(s+1.077\times10^7)(s+8.609\times10^6)(s+5.054\times10^6)(s+1.665\times10^6)(s+1.113\times10^5)}, \\ \frac{\hat{v}_o(s)}{-\hat{i}_{load}(s)} = \frac{3.74(s+1.077\times10^7)(s+8.61\times10^6)(s+5.056\times10^6)(s+1.669\times10^6)(s+1.318\times10^5)}{(s+1.077\times10^7)(s+8.609\times10^6)(s+5.054\times10^6)(s+1.665\times10^6)(s+1.113\times10^5)}. \end{cases} \tag{5.43}$$

steady-state errors in the output voltage during step changes in the input voltage and load current.

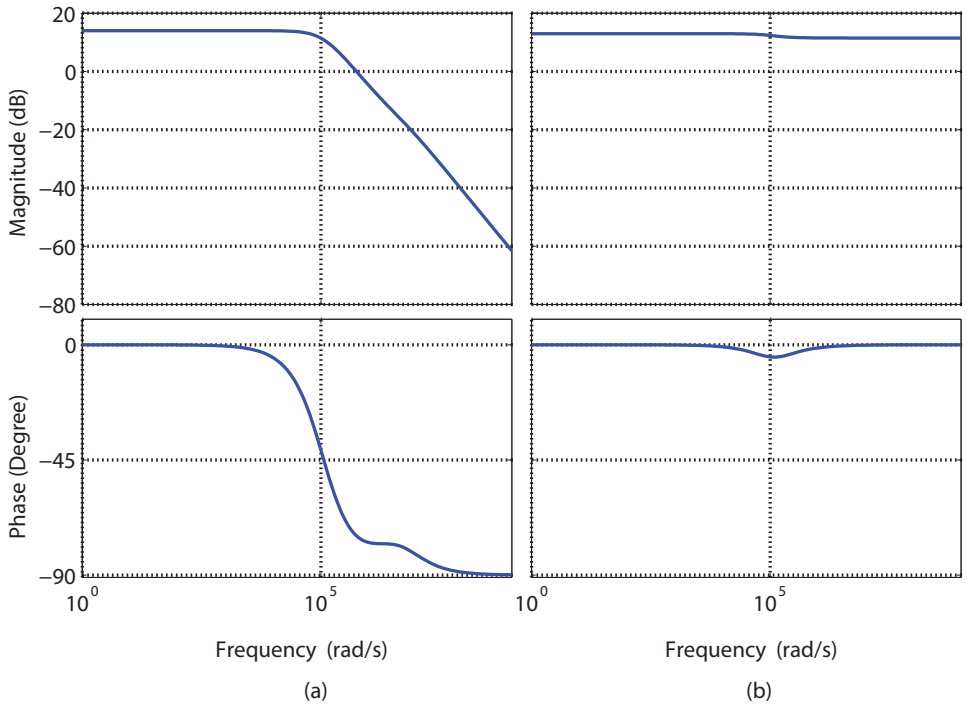


Figure 5.12: Frequency response of the output voltage of the open-loop MMC3 with (a) input voltage and (b) load current.

5.4.2 Transfer Function of the System with the Proposed Control

To embed the proposed control in the MMC3 model, the small-signal model in (5.42) is first updated with m_a index as a new input to the system, i.e., $u = [v_{lv} - V_d; -i_{load}; m_a]$

$$\begin{cases} \frac{\hat{v}_o(s)}{\hat{v}_{lv}(s)} = \frac{10^6 s(s+1.028\times10^7)(s+8.752\times10^6)(s+3.926\times10^6)(s+1.475\times10^6)}{(s+1.095\times10^7)(s+8.997\times10^6)(s+5.313\times10^6)(s+1.774\times10^6)(s+1.038\times10^5)(s+71.36)}, \\ \frac{\hat{v}_o(s)}{-\hat{i}_{load}(s)} = \frac{7.2727s(s+1.096\times10^7)(s+8.981\times10^6)(s+5.334\times10^6)(s+1.756\times10^6)(s+1.236\times10^5)}{(s+1.095\times10^7)(s+8.997\times10^6)(s+5.313\times10^6)(s+1.774\times10^6)(s+1.038\times10^5)(s+71.36)}. \end{cases} \tag{5.47}$$

and $m_a = M_a + \hat{m}_a$. By linearization of the small-signal model, we deduce

$$\begin{cases} \dot{\hat{x}} = (\frac{2-M_a}{2}A_1 + \frac{M_a}{2}A_2)\hat{x} + (\frac{2-M_a}{2}B_1 + \frac{M_a}{2}B_2)[\hat{v_{lv}}, -\hat{i_{load}}] \\ + [-\frac{1}{2}(A_1X + B_1[V_{lv}; -I_{load}]) + \frac{1}{2}(A_2X + B_2[V_{lv}; -I_{load}])]\hat{m}_a, \\ \hat{y} = (\frac{2-M_a}{2}C_1 + \frac{M_a}{2}C_2)\hat{x} + (\frac{2-M_a}{2}D_1 + \frac{M_a}{2}D_2)[\hat{v_{lv}}, -\hat{i_{load}}] \\ + [-\frac{1}{2}(C_1X + D_1[V_{lv}; -I_{load}]) + \frac{1}{2}(C_2X + D_2[V_{lv}; -I_{load}])]\hat{m}_a. \end{cases} \tag{5.44}$$

Then, to embed the proposed feedback control in the model, two additional states are introduced:

$$\begin{cases} \dot{z} = r - y, \\ \dot{r} = 0, \end{cases} \tag{5.45}$$

where r is the reference for the output voltage and is constant. m_a index is calculated by

$$\hat{m}_a = K_p(r - y) - K_i z, \tag{5.46}$$

where the proportional gain K_p and integral gain K_i are specified in Table 5.1. By substituting (5.46) into (5.44), the small-signal state-space model of the MMC3 with the proposed control is derived. The transfer functions of the closed-loop MMC3 system are given in (5.47).

The Bode diagrams of the closed-loop system are given in Fig. 5.13. Unlike the open-loop system, $\hat{v}_o(s)/\hat{v}_{lv}(s)$ and $\hat{v}_o(s)/(-\hat{i}_{load}(s))$ demonstrate significantly reduced gain magnitude at low frequencies, which allows the system to eliminate steady state errors in the output voltage during step changes in the input voltage and load current.

The output voltage response to step changes in the load current for both the open-loop and closed-loop MMC3 based on the derived transfer functions and parameters in Table

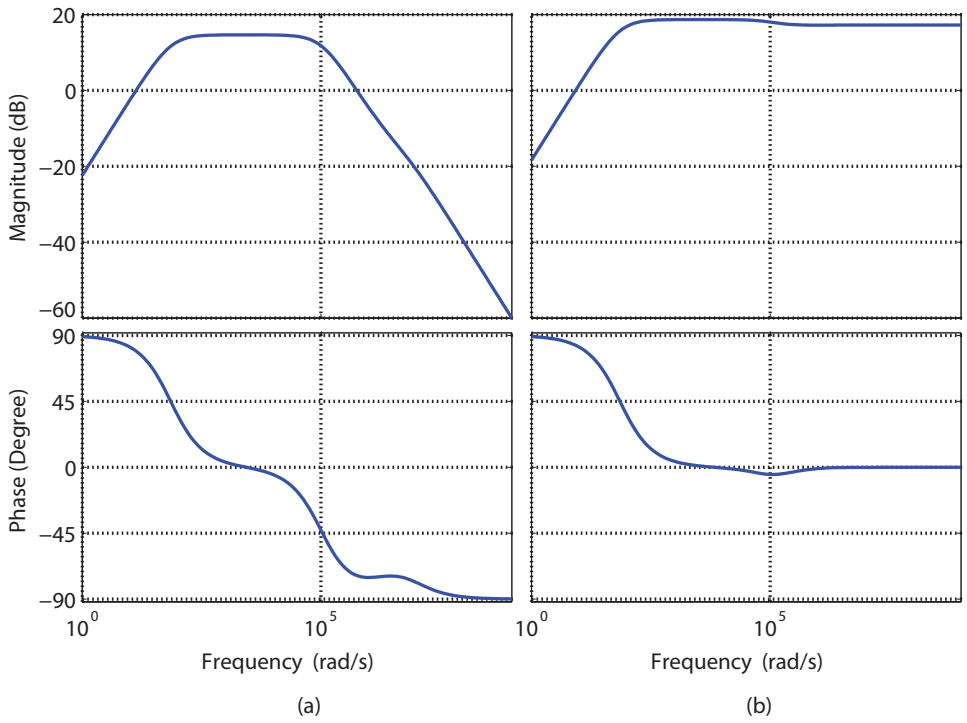


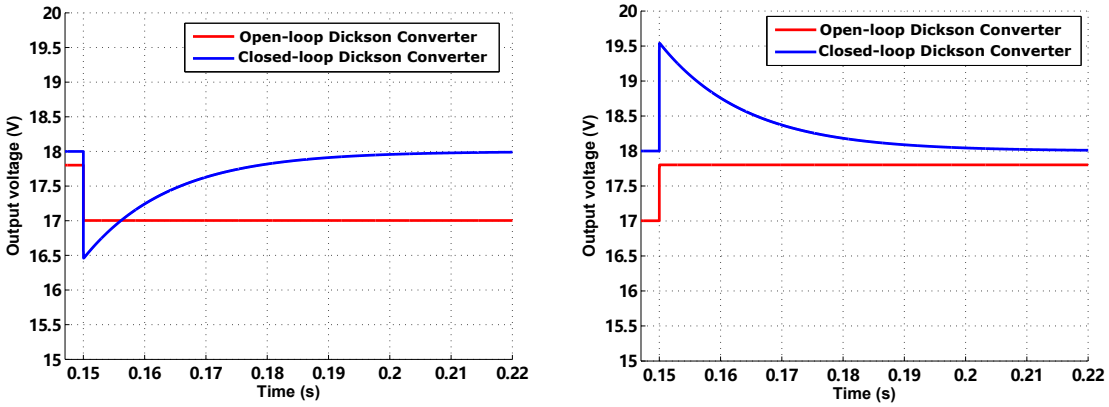
Figure 5.13: Frequency response of the output voltage of the closed-loop MMC3 with (a) input voltage and (b) load current.

5.1 is demonstrated in Fig. 5.14. The load resistance is decreased from $100\ \Omega$ to $50\ \Omega$ in Fig. 5.14(a) and increased from $50\ \Omega$ to $100\ \Omega$ in Fig. 5.14(b). The results clearly demonstrate that the open-loop MMC3 cannot maintain the output voltage during load transients while the MMC3 with the proposed control strategy is able to properly maintain and regulate the output voltage.

5.5 Simulation Results

The MMC3 of Fig. 5.2 is simulated using LTSPICE. Key parameters of the study system are listed in Table 5.2. The parasitic inductance in one SM is measured to be around 100 nH using an impedance analyzer on the fabricated MMC3 prototype. The switching frequency is thus selected to be 335 kHz based on the following parameters and equation (5.29) to realize full ZCS for the power devices.

The voltages of the output and each SMs of the study system are given in Fig. 5.15



(a) (b)

Figure 5.14: Output voltage response of the open-loop and the closed-loop MMC3 to (a) a step increase and (b) a step decrease in the load current based on the derived transfer functions.

and the key waveforms of switch S6 as in Fig. 5.3 are plotted in Fig. 5.16. Based on the time-domain model of the MMC3, the voltages and currents are calculated theoretically according to equations (5.21) and (5.27) and system parameters provided in Table 5.3 for comparison.

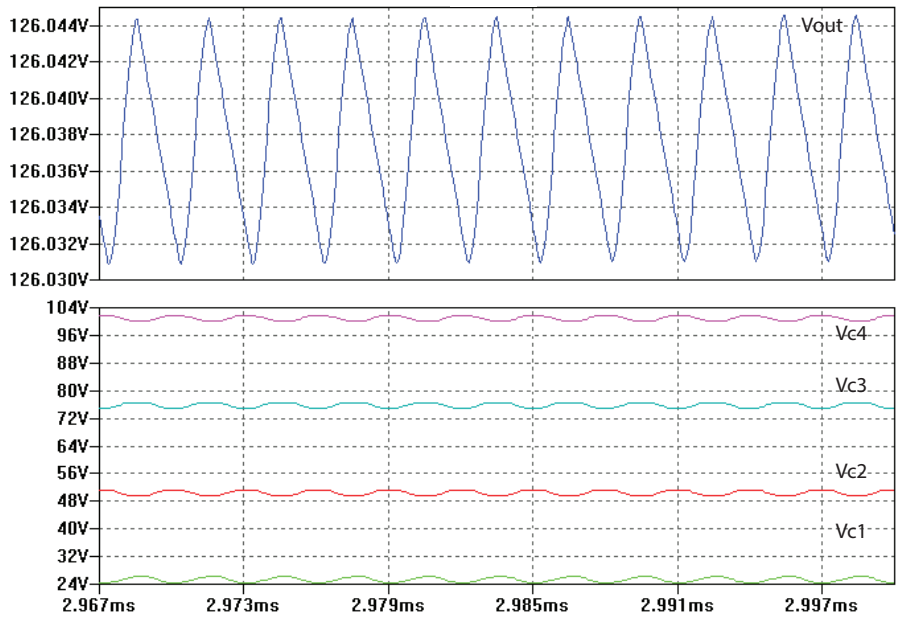


Figure 5.15: Output voltage and capacitor voltage of last SM in the simulated MMC3 system.

Table 5.2: Parameters of the study system

Parameter	Value
Input voltage	26 V
Output resistance	100 Ω
Total number of SMs	4
Switching frequency	335 kHz
Deadtime	250 ns
SM capacitance	2.2 uF
SM inductance	100 nH
Output capacitance	165 uF
Switch on-resistance	30 mΩ
Diode on-resistance	30 mΩ
Capacitor equivalent series resistance	80 mΩ
Diode forward voltage drop	0.4 V

Table 5.3: Comparison of simulation results and the time-domain model

Parameter	Simulation	Model
Output voltage	126 V	124.5 V
Output voltage ripple	0.013 V	0.011 V
SM 1 capacitor voltage	25.3 V	25.29 V
SM 2 capacitor voltage	50.45 V	50.58 V
SM 4 capacitor voltage	100.89 V	101.16 V
SM capacitor voltage ripple	1.68 V	1.66 V
SM capacitor peak current	5.5 A	5.00 A
Switch current RMS	2.29 A	2.50 A

Based on Table 5.3 and Figs. 5.15 and 5.16, the time-domain model is proved to provide very accurate results for the key values of the MMC3 performance. ZCS turn-on and turn-off are clearly observed for the power switches. The voltage ripple associated with each SM capacitor is the same as proved in the previous sections.

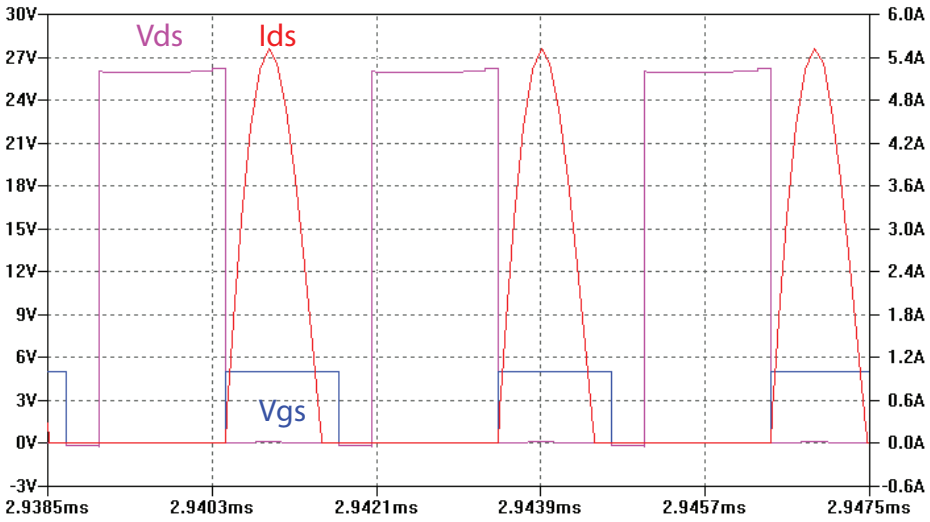


Figure 5.16: Capacitor voltage and current of (a) and (b) SM 1 and (c) and (d) SM 2 in the simulated MMC3 system.

CHAPTER 6
DESIGN OF A DICKSON CONVERTER PROTOTYPE

After understanding the operating principles and proposing a closed-loop voltage control strategy for the MMC3, an MMC3 prototype is built to demonstrate the advantages of the system and to validate the proposed control. As the Dickson converter shares the same operating principle as the MMC3 while features a simpler control implementation, it is selected for prototype design. In this chapter, the process of selecting power devices, passive components and the switching frequency is presented. Tradeoffs and comparisons are made between different operating modes and a multi-objective optimal design of the Dickson converter is demonstrated with simulation results. The main system input-outupt specifications listed in Table 6.1 are used for prototype design.

Table 6.1: System specifications of the Dickson converter prototype

Parameter	Value
Input voltage	26 V
Output voltage	125 V
Output power	160 W
Output resistance	100 Ω
Total number of SMs	4
Parasitic inductance	100 nH

6.1 Selection of Power Devices

As the input voltage of the system is at maximum 26 V, for the Dickson converter system, the power switches rated at 40 V can be used, while the power diodes should be rated at twice the input voltage. The current rating of power devices are determined as 5 A based on the simulation results in Section 5.5. In order to pick the power devices that are best suited

for the system, a device pool is formed with several state-of-the-art power devices rated to 40 V consisting of both GaN FETs and Si MOSFETs. A comparison of the on-state resistance, gate charge and output charge of the selected devices is demonstrated in Fig. 6.1. These parameters can serve as figures of merits when comparing power devices and the smaller their values are, the lower conduction and switching losses will be. From the comparison, it is evident that the GaN power devices have much less gate charge and output charge compared with similarly-rated Si devices, leading to smaller switching losses. On the other hand, the on-state resistance of GaN devices may not be necessarily smaller than their Si counterparts. In the Dickson converter system as ZCS operation is available, devices with lower on-state resistance and output charge will be most favorable.

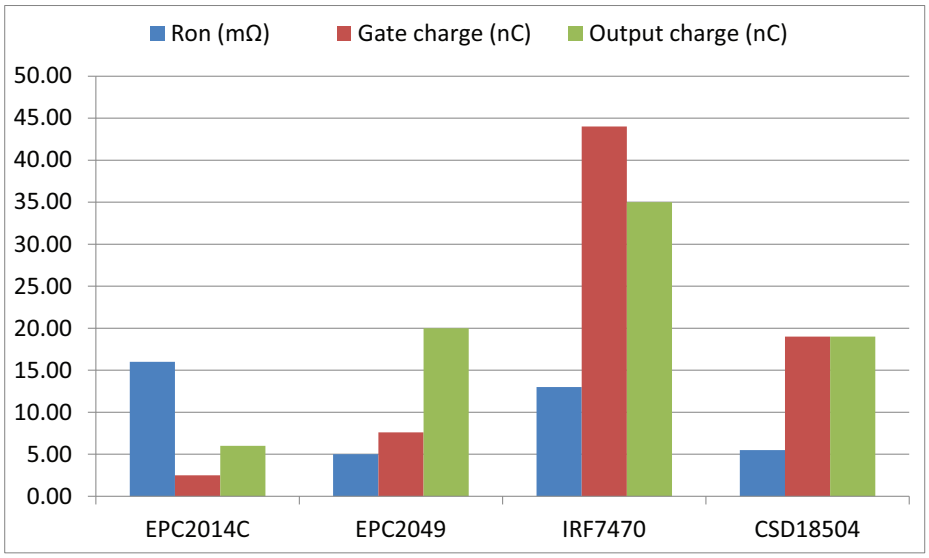


Figure 6.1: Comparison of selected power devices.

A similar device pool has been built for power diodes rated at 100 V and 5 A as shown in Fig. 6.2. The voltage ratings of the diodes are selected slightly higher as the 100 V diodes turn out to have better forward characteristics. The power loss generated by 3 A DC current available in the datasheets is selected as the criteria for comparison as the reverse recovery of diodes is avoided by maintaining ZCS. Based on Fig. 6.2, the diode SDT5H100P5 has a superior loss performance than others and is thus selected for this prototype design.

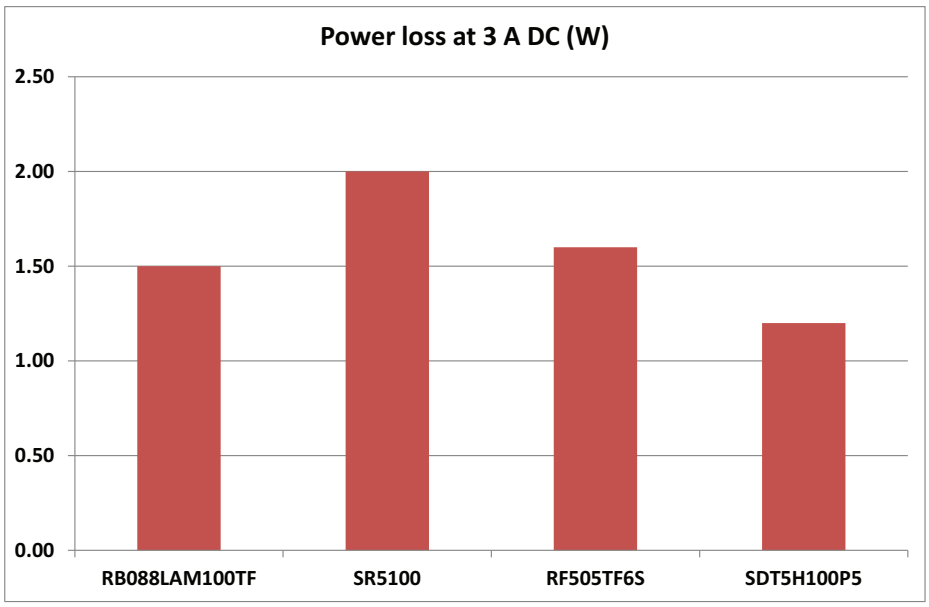


Figure 6.2: Comparison of selected power diodes.

6.2 ZCS Operation

In the previous chapter, the possibility of realizing ZCS with the help of parasitic inductance is discussed. However, it is desired to know how parasitic inductance will affect the capacitor current waveform and the power losses of the converter. Fig. 6.3 demonstrates the change in capacitor current waveform brought by the parasitic inductance in the loop. The results are based on simulation of the circuit in Fig. 6.4 with the parameters listed in Table 6.2.

Table 6.2: Parameters of the study system

Parameter	Value
Input voltage	26 V
Capacitor voltage pk-pk ripple	1 V
Switching frequency	335 kHz
Deadtime	250 ns
SM capacitance	2.2 uF
Switch on-resistance	30 mΩ
Diode on-resistance	30 mΩ
Diode forward voltage drop	0.4 V

As shown in Fig. 6.3, by proper selection of the switching frequency, no matter whether

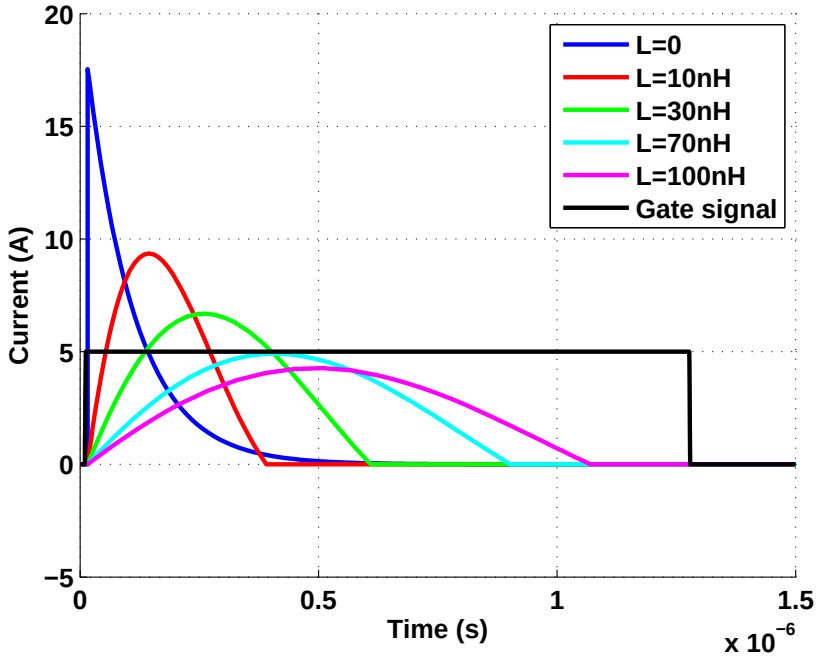


Figure 6.3: Capacitor current under different parasitic inductance values.

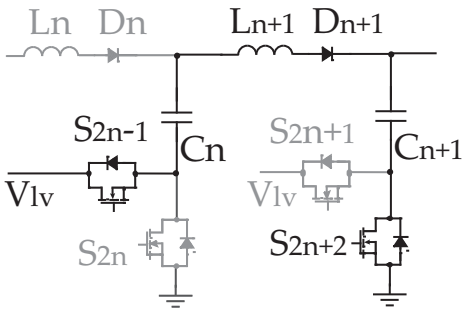


Figure 6.4: Parasitic inductance between the SMs of the Dickson converter.

the capacitor current is over-damped or under-damped, ZCS switching can be guaranteed. However, with a larger parasitic inductance, the peak current is reduced and therefore, so is the current RMS, thus reducing the current rating requirement and conduction losses. However, the system will suffer from unnecessary losses if the deadtime is set too long. It is desirable to adjust the deadtime at its minimum requirement and turn the device off right after its current becomes zero to maintain ZCS operation.

6.3 Cross-talk Protection

The basics of cross-talk issue was introduced in Section 2.1 through an example with a half-bridge configuration feeding an inductive load. In the Dickson converter, a typical switching transient between two interconnected SMs is used to analyze the cross-talk problem. The circuit diagram of the transient is shown in Fig. 6.5. In this transient, switch S_1 and S_3 are being turned on while S_2 has already been turned off, and a positive voltage surge may be observed at the gate terminal of S_2. A simulation model of this circuit has been built in the LTSPICE with the main parameters listed in Table 6.3. As the simulation is mainly used to analyze cross-talk problem in the circuit, the equivalent model of MOSFET in Fig. 2.1 introduced in Section 2.1 is used. The simulated circuit diagram is shown in Fig. 6.7. A GaN power device, EPC2034, is used as an example for this analysis. The parasitic capacitance values of this device depend much on the drain-source voltage as shown in Fig. 6.6. One important thing to note here is that in the Dickson converter system, according to the analysis in Section 5.2, the drain current of S_2 will be zero when it turns off due to the ZCS operation. Thus, no current is available to charge the C_{ds} of S_2, and S_2 will block zero voltage until S_1 turns on. In this sense, since the focus is on the gate-source voltage transient of S_2, which is already off at this switching transient moment, the parasitic capacitance values used in Table 6.3 are corresponding to those at $V_{ds} = 0$ in Fig. 6.6. The initial voltage of capacitors C_1 and C_2 are assumed to be V_{lv} and $(2V_{lv} - 2)$, respectively.

The simulation result is shown in Fig. 6.8. The gate-source voltage of S_2 is shown in the upper plot while the gate-source voltage of S_1, the inductor current and drain-source voltage of S_2 are shown at the bottom. At the turn-on instant of S_1, S_2 has already turned off. However, there is still a positive surge voltage of 1.2 V showing up at the gate terminal of S_2. For the EPC2034 GaN devices, the turn-on threshold voltage is in the range of 0.8 V to 2.5 V, typically 1.4 V [70]. In this case, the surge voltage due to cross-talk can very likely

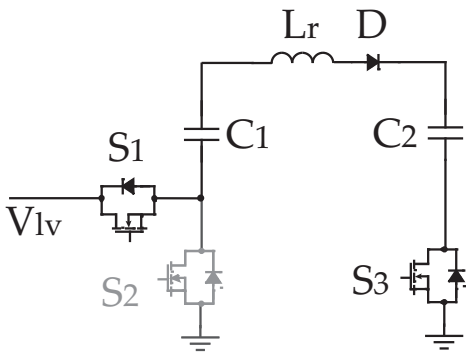


Figure 6.5: Switching transient in Dickson converter for cross-talk analysis.

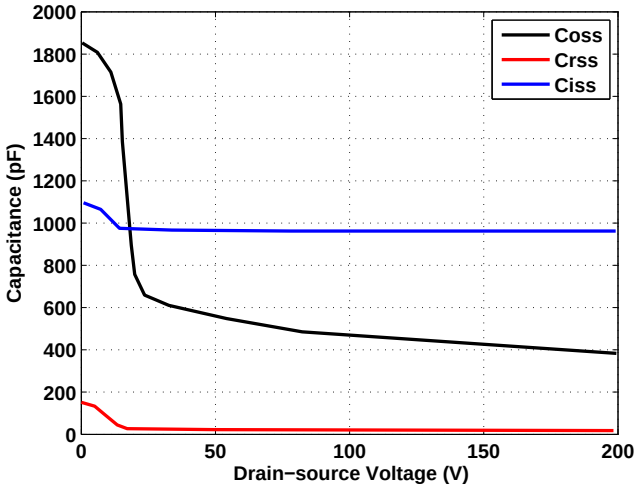


Figure 6.6: Parasitic capacitances of EPC2034 [70].

lead to a shoot-through between S_1 and S_2, causing a large current through the devices and possibly damaging them.

On the other hand, as ZCS is present in the Dickson converter, there is no load current that free-wheels through the devices as shown in Fig. 6.8, and the cross-talk effect during the turn-off of power devices is much reduced. Thus, the analysis only focuses on the cross-talk during device turn-on.

To deal with the cross-talk problem, the most straightforward way is to put an external capacitor between the gate-source terminal of the device as shown in Fig. 6.9. The simulation result with a 15 nF external capacitor connected is shown in Fig. 6.10. As shown, the cross-talk effect has been largely suppressed. However, as the external capacitor is direcly

Table 6.3: Parameters of the cross-talk simulation

Parameter	Value
Input voltage	26 V
Switching frequency	335 kHz
Deadtime	250 ns
V_{gs}	5 V
C_{gs}	1 nF
C_{gd}	130 pF
C_{ds}	1 nF
C_{drive}	2.2 uF
$R_{gs,on}$	4.1 Ω
$R_{gs,off}$	0.6 Ω
C_1, C_2	2.2 uF
L_r	100 nH
Switch $R_{ds,on}$	30 mΩ
Diode on-resistance	30 mΩ
Diode forward voltage drop	0.4 V
Capacitor equivalent series resistance	80 mΩ

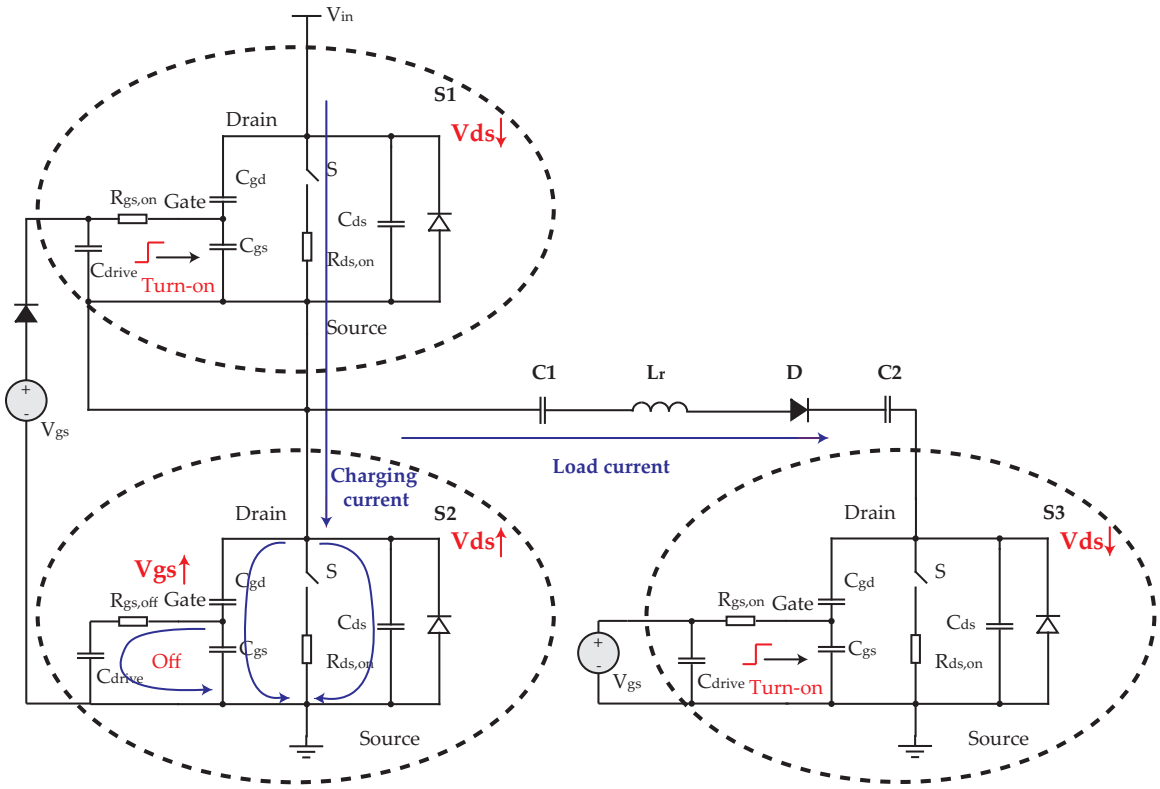


Figure 6.7: Simulation circuit in the LTSPICE for cross-talk analysis.

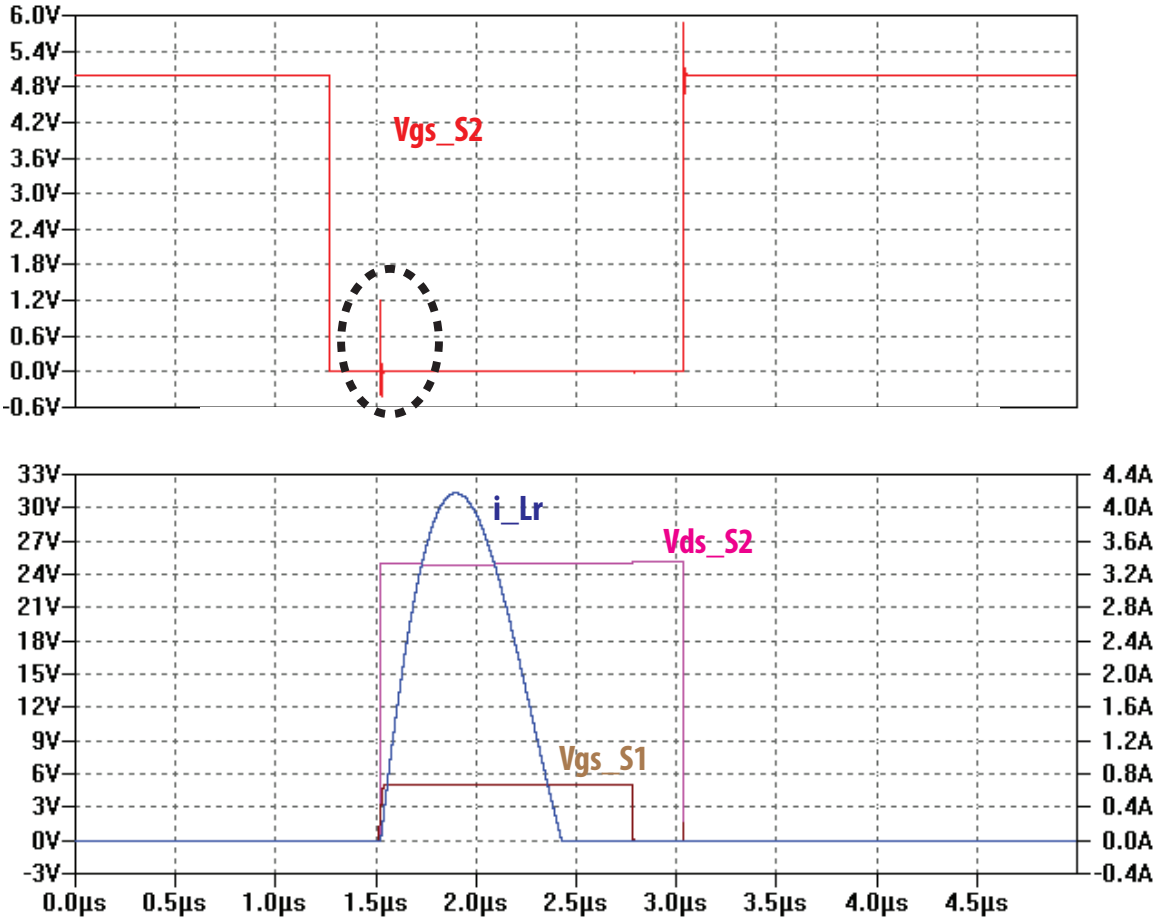


Figure 6.8: Simulation waveforms showing the cross-talk effect on S_2.

in parallel with C_{gs}, during the turn-on process of the device, the gate driver circuit needs to charge both capacitors, leading to much larger gate drive losses. Thus, an active gate driver as proposed in [23], which avoids the additional loss brought by a low-impedance path during the turn-on transient is preferred to solve this problem.

6.4 Optimal Design of the Dickson converter

Based on the previous analysis, a multi-objective optimal design problem can be formed to select the remaining design parameters for the Dickson converter. The objectives of the optimal design problem are system efficiency and output voltage ripple. The variables are selection of power device, SM and output capacitance and switching frequency.

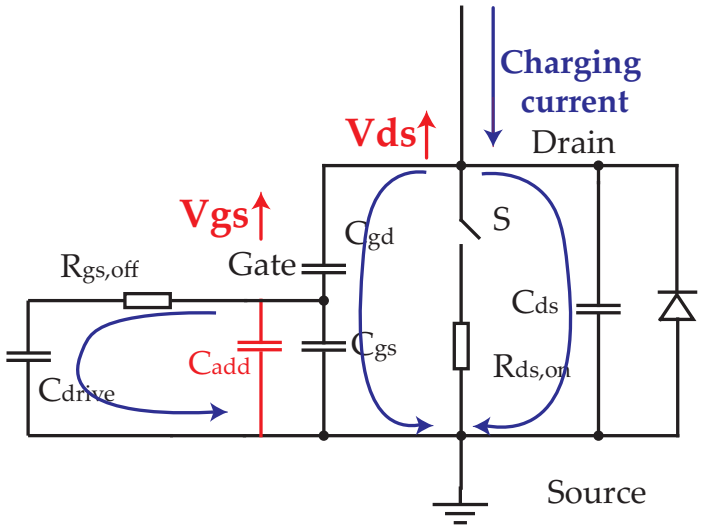


Figure 6.9: External gate capacitor added to suppress the cross-talk effect.

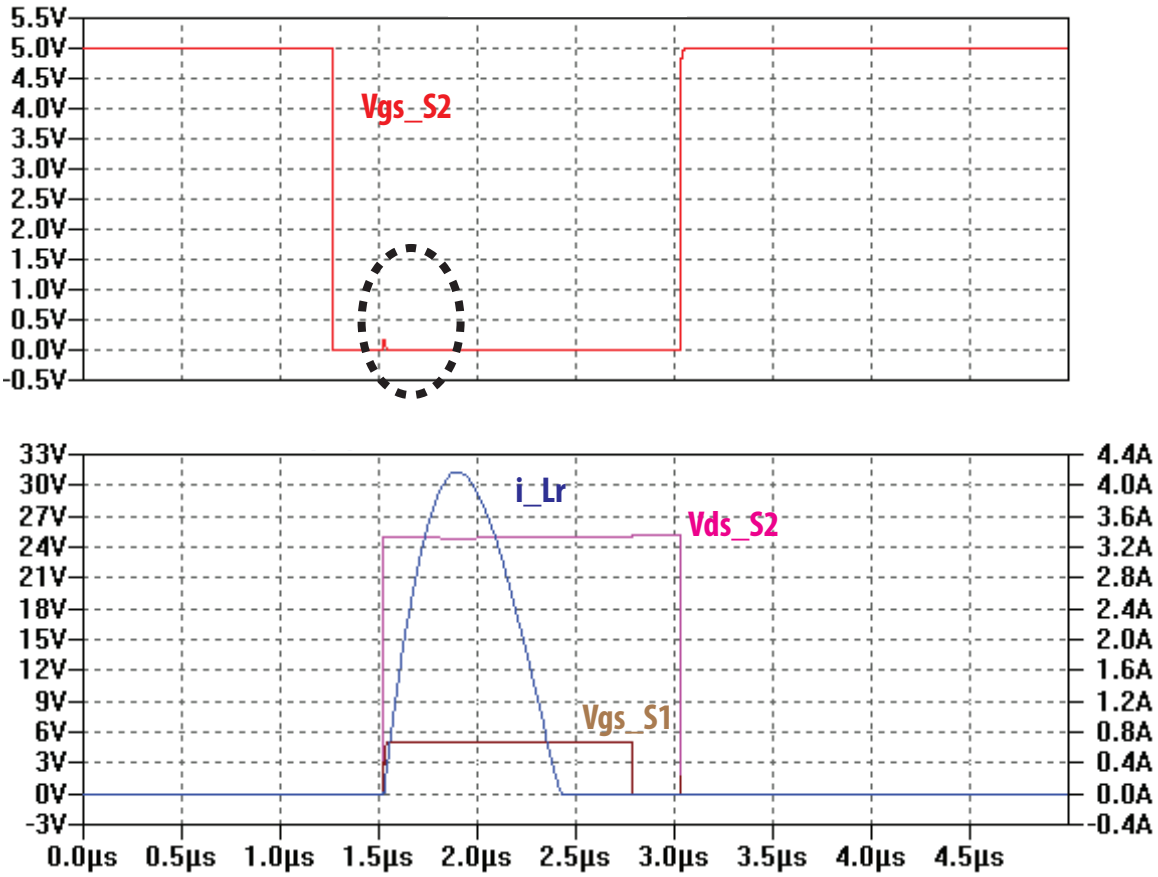


Figure 6.10: Simulation waveforms showing the cross-talk effect on S_2 suppressed by adding an external capacitor.

The optimization is performed by sweeping through all possible values within their reasonable ranges and comparing the objective values achieved by every combination of design parameter values. To avoid evaluating the combinations that lead to a system with poor performance, several constraints are set up to eliminate system designs that i) cannot meet the output requirement, ii) lose ZCS operation, and iii) fail to achieve 90% system efficiency and 0.1 V pk-pk output voltage ripple.

By solving the optimal design problem in MATLAB, a Pareto front can be found in Fig. 6.11, where every blue circle represents a viable design that satisfies all constraints. One design with relatively high peak efficiency of 96.5% and output ripple of 0.07 V, as highlighted in red in Fig. 6.11, is selected. The design parameters of the selected design are listed in Table 6.4 and its efficiency curve is plotted against output power in Fig. 6.12. A detailed power loss breakdown is shown in Fig. 6.13.

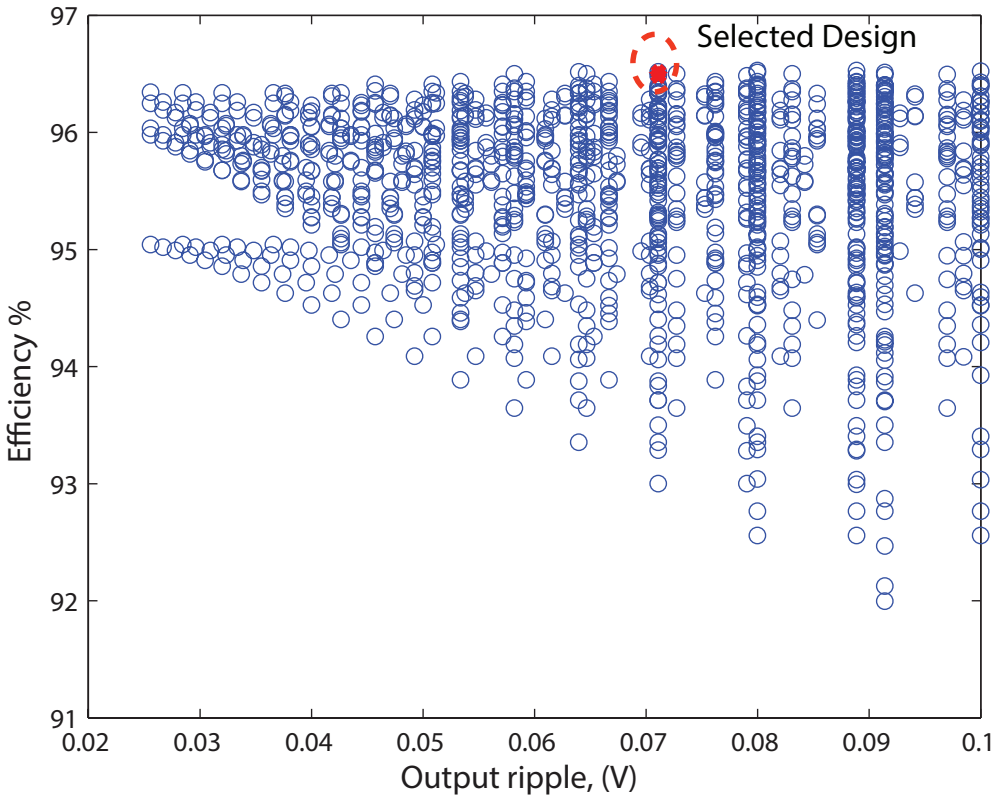


Figure 6.11: Viable designs of the Dickson converter.

Table 6.4: Parameters of the selected design

Parameter	Value
Switching frequency	200 kHz
Power Device	EPC 2049
Power Diode	SDT5H100P5
C_{out}	100 uF
C_{SM}	6 uF

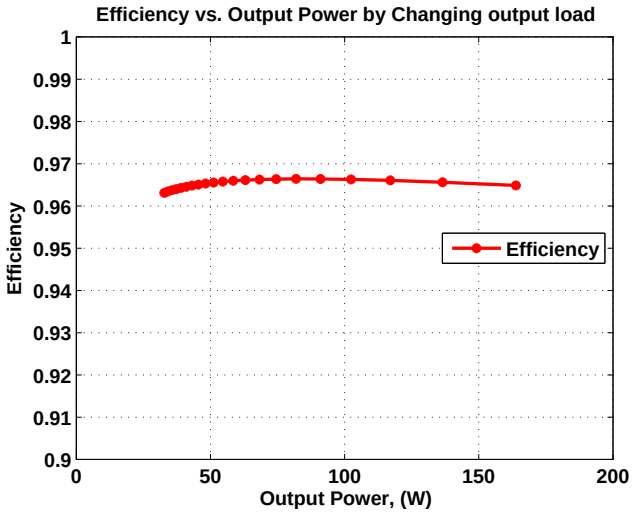


Figure 6.12: Efficiency curve of the selected design.

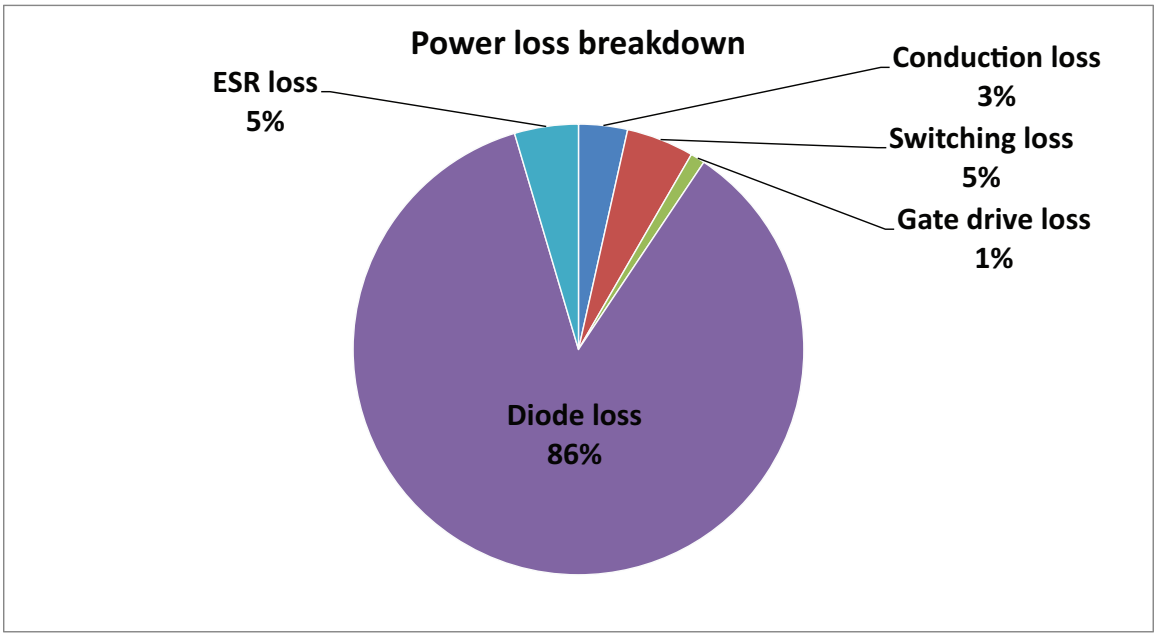


Figure 6.13: Power loss breakdown of the selected design.

CHAPTER 7
EXPERIMENTAL RESULTS

7.1 Experiment Setup

To experimentally validate the developed time-domain model and evaluate the performance of the proposed control strategy, a converter prototype based on GaN FETs is implemented. The developed prototype is shown in Fig. 7.1. The component specifications are listed in Table 7.1 while the main parameters of the system are listed in Table 7.2. The control strategy is implemented in a TI F28069 microcontroller. The test setup is shown in Fig. 7.2.

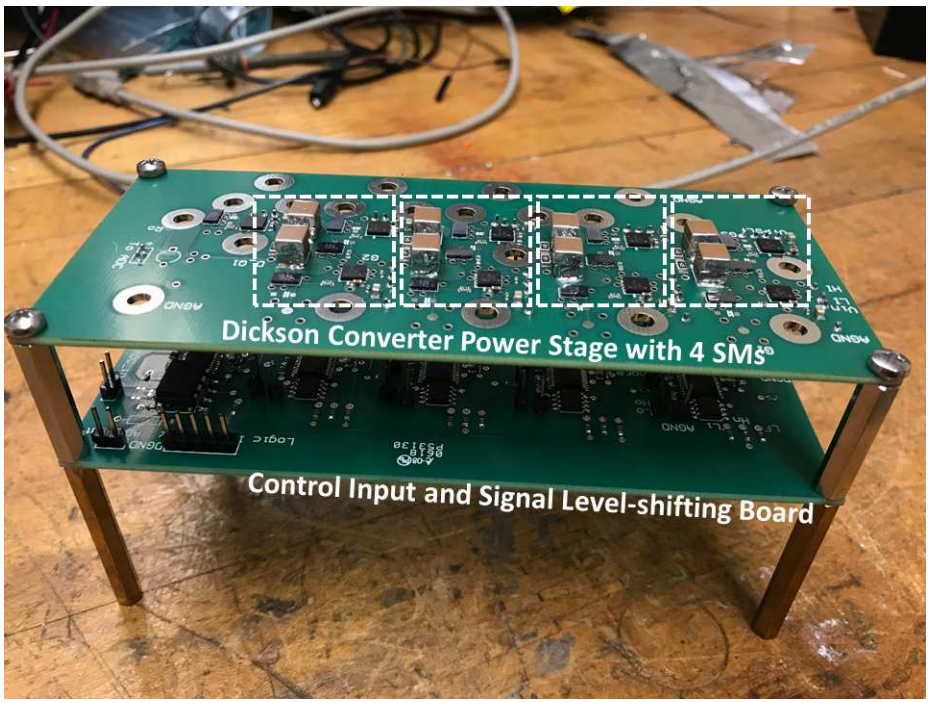


Figure 7.1: The converter prototype with the power stage (top) and signal/control stage (bottom).

Table 7.1: List of components used for the Dickson converter prototype

Component	Part number	Ratings
Power switches	EPC2034	200 V, 48 A
Diodes	SR5100	100 V, 5 A
SM capacitor	C5750X6S2W225K250KA	450 V, 2.2 uF
Gate driver IC	LM5113	
Digital Isolator	SI8423BB-D-IS-ND	
Level shifter	ADUM5210ARSZ-ND	

Table 7.2: Parameters of the study system

Parameter	Value
Input voltage	26 V
Output resistance	100 Ω
Total number of SMs	4
Switching frequency	335 kHz
Deadtime	250 ns
SM capacitance	2.2 uF
SM inductance	100 nH
Output capacitance	165 uF
Switch on-resistance	30 mΩ
Diode on-resistance	30 mΩ
Capacitor equivalent series resistance	80 mΩ
Diode forward voltage drop	0.4 V

7.2 Key Waveforms

The waveforms of switch S_6 of the Dickson converter as in Fig. 5.3 obtained with the operating condition listed in Table 7.2 are shown in Fig. 7.3. The drain-source voltage and current of the GaN devices are closely aligned with the theoretical values and the simulated waveform in Fig. 5.16. The ZCS operation during both turn-on and turn-off transitions is observed. The output voltage is measured to be 124.9 V, which is closely matched with the theoretical value of 124.5 V calculated based on the time-domain model of the converter.

The transients of insertion/bypass of SM1 during operation are also captured and the key waveforms are presented in Fig. 7.4. When SM1 is bypassed, the conversion ratio of the system decreases and the output voltage and other SM capacitor voltages become

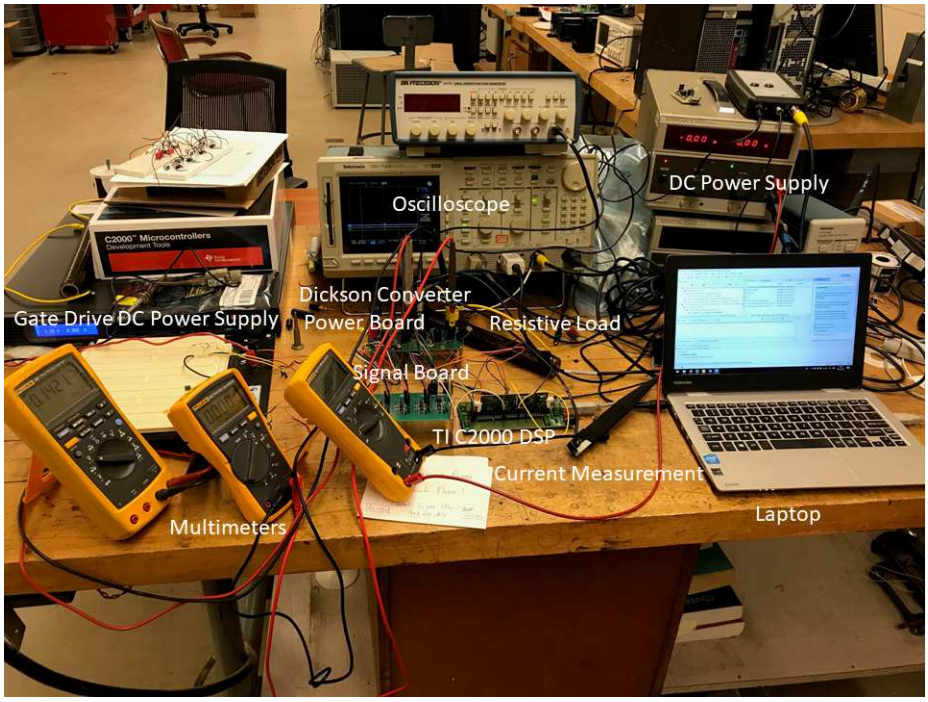


Figure 7.2: Test setup with the Dickson converter prototype.

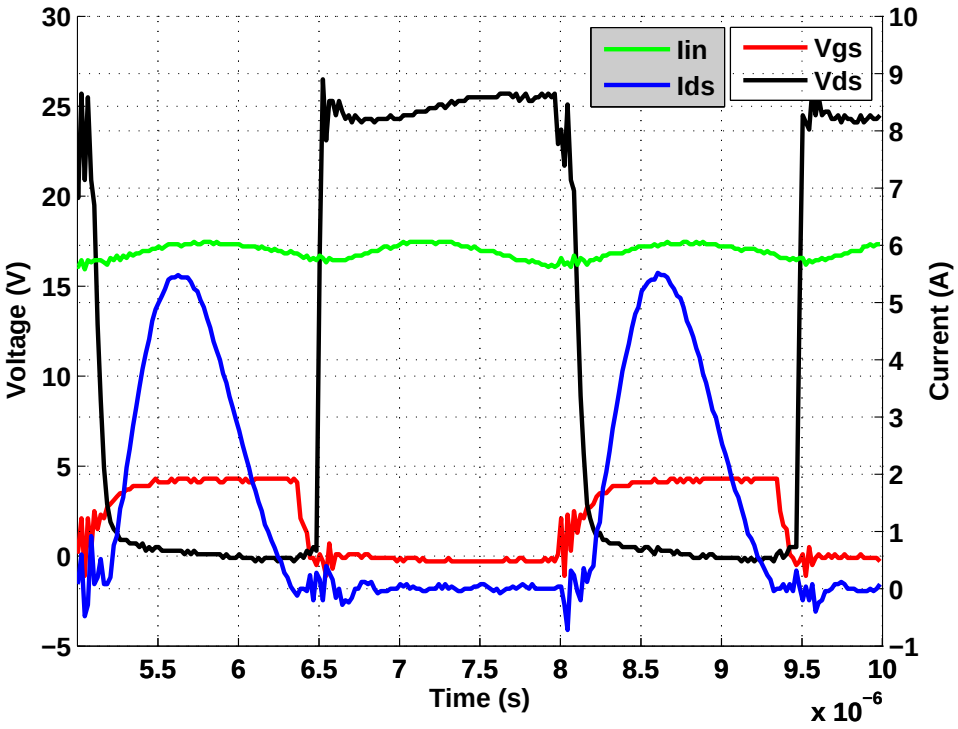


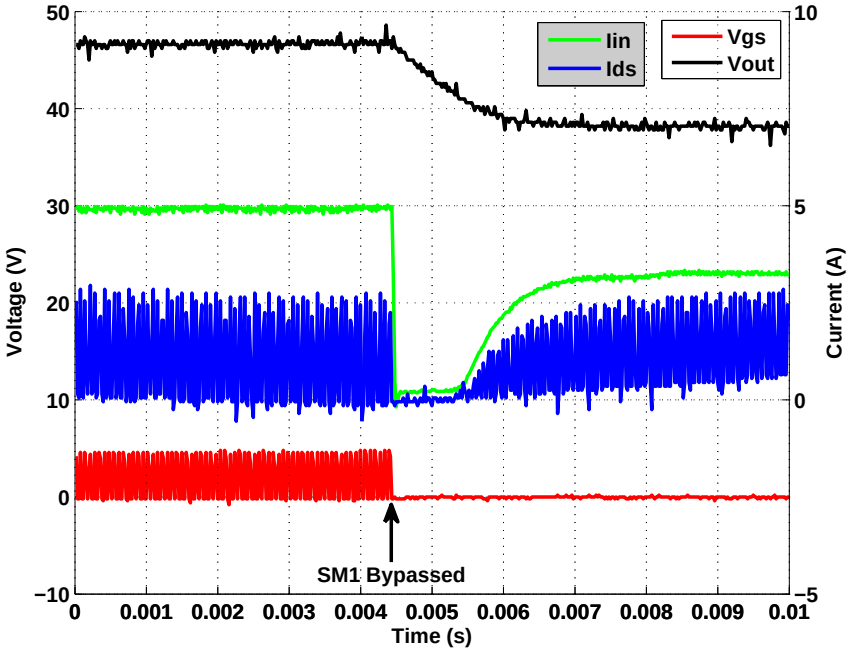
Figure 7.3: Key waveforms of the converter operating with 26 V input and 100 Ωload at 335 kHz.

higher than the new steady-state values. Thus, the input current to the system is greatly reduced and the current in the system is lower than its value under normal operation until the output and other SM capacitors get discharged through the load to the new steady state of a 3-SM system. On the contrary, when SM1 is inserted, a significant increase in the current is observed due to charging of the capacitors to the new steady-state values of a 4-SM system.

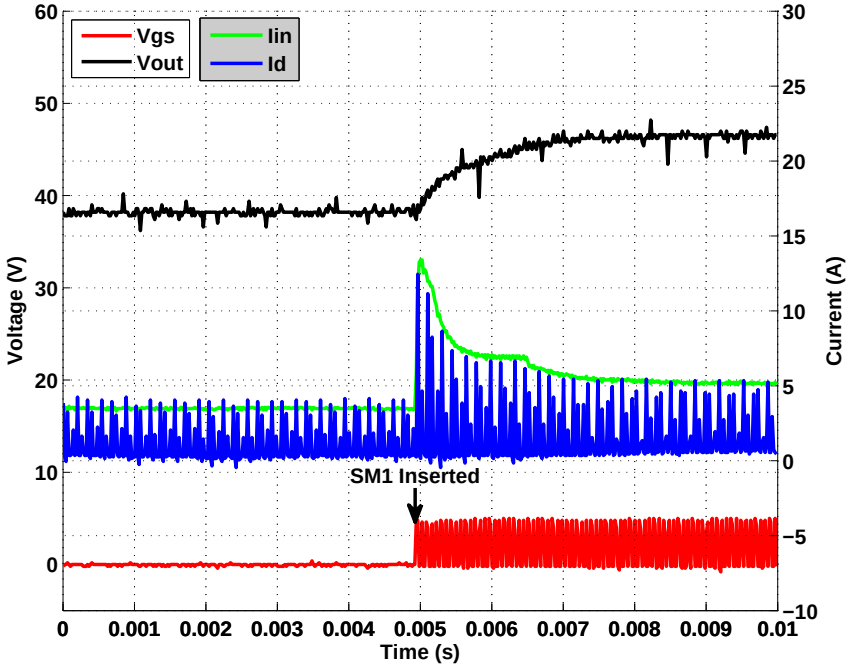
7.3 System Efficiency and Power Loss Analysis

The efficiency of the converter with 3 or 4 inserted SMs is calculated as in Fig. 7.5(a). The 4-SM system is tested up to 170 W output power and achieves an efficiency of 91.5%, and 93.8% considering only the power stage. A power loss analysis is conducted for the 4-SM converter, which is shown in Fig. 7.5(b). Majority portion of the power losses in the system originates from multiple gate drive and level-shifting devices for the 8 GaN FETs and conduction losses of the diodes. The switching losses are very small due to the ZCS operation of power devices.

Compared with the power loss profile of the optimal design analyzed in Section 6.4, the prototype has much more gate drive losses. One reason is that a 15 nF external capacitor is connected to the gate-source terminal of each GaN device to protect the devices from cross-talk effect as mentioned in Section 6.3. This leads to a significant increase in the gate charge of device and thus induce more gate drive loss. However, the high gate drive loss measured is still not expected. The gate drive loss included here is directly calculated by the readings on the gate drive power supply, which may have errors or include losses on wires, etc. Thus, a more reasonable evaluation might be looking at the power stage efficiency excluding the gate drive and auxillary circuit losses. In that case, the power stage efficiency of the system is 93.8%. The system efficiency can be further improved by using the power devices selected in Table 6.4, which can lead to greatly reduced conduction losses, and shorten the deadtime to achieve a lower SM capacitor current.

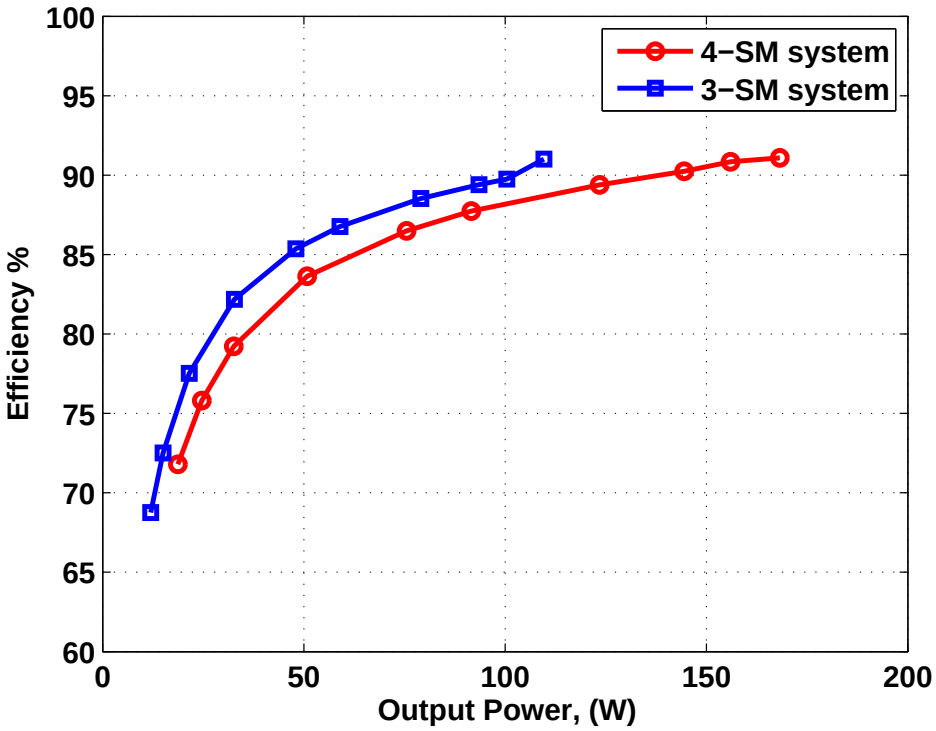


(a)

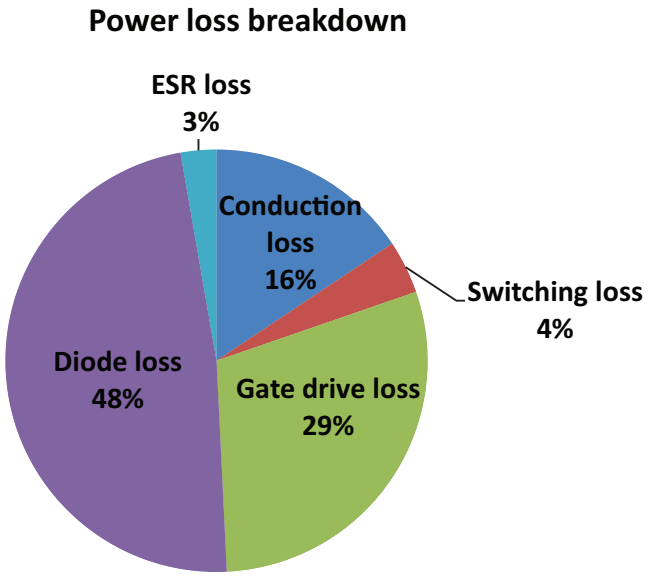


(b)

Figure 7.4: Output voltage, input current, switch S6 current and SM1 gate signal during (a) bypass and (b) insertion of SM1.



(a)



(b)

Figure 7.5: (a) Efficiency of the converter with 3 and 4 SMs and (b) power loss analysis for the 4-SM converter with 26 V input voltage and 100 Ω output load.

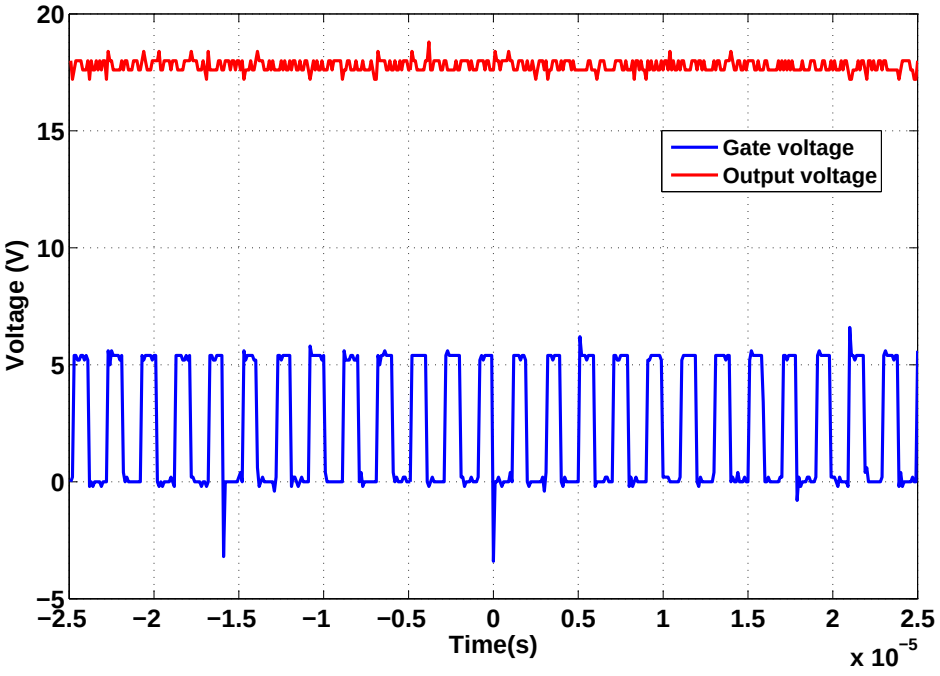
7.4 Validation of the Proposed Control Strategy

Experiments are carried out with 5 V input voltage, 18.8 V output voltage reference and a 100 Ω load. While in the open-loop system, the output voltage will change as the input voltage changes, in the closed-loop system, as shown in Fig. 7.6(a) and (b), when the input voltage is increased from 4.42 V to 5.02 V, the output voltage still accurately tracks the reference voltage by adjusting m_a. This verifies the effectiveness of the proposed strategy to reject source voltage disturbance. Figures 7.7(a) and (b) show the output voltage of the MMC3 under the PDT feedback and open-loop control strategies, respectively, during the same load-change scenarios in Fig. 5.14. As shown, the output voltage in the open-loop case changes during a load-change and the system is not able to return to its previous setpoint. On the contrary, in both cases, the system with the proposed control strategy is able to maintain the output voltage regulated within 0.1 s. The experimental results align well with the simulation results in Fig. 5.14.

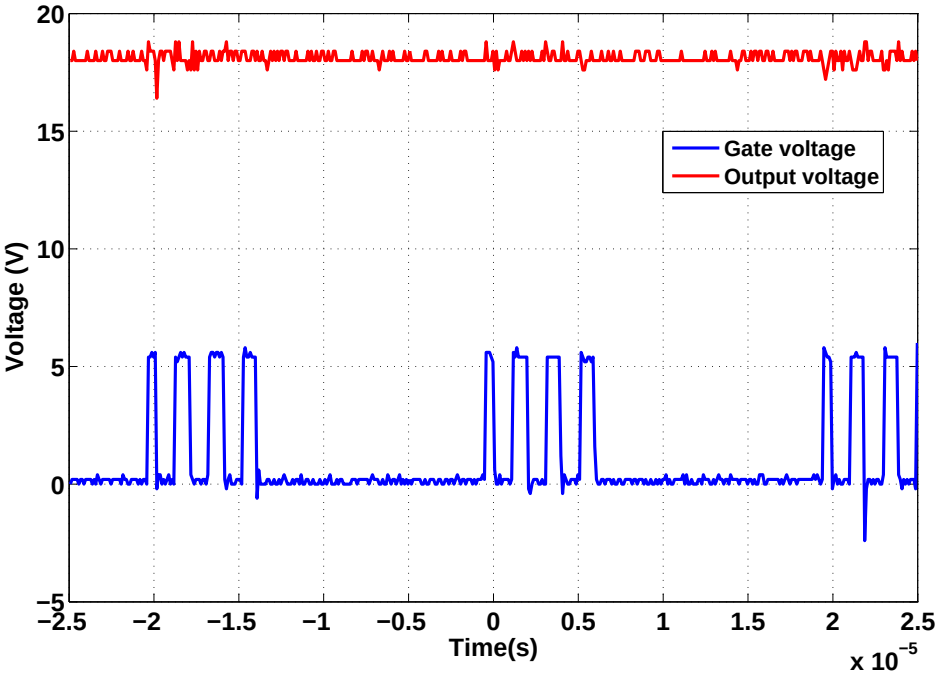
In order to evaluate the proposed control strategy with a higher output voltage and power, the prototype is tested with 50 V output voltage reference, load resistance decreasing from 50 Ω to 33 Ω and input voltage increasing from 11 V to 15 V. The system was able to regulate the output voltage at the reference value despite both load- and source-side disturbances as shown in Fig. 7.8.

7.5 Efficiency and Ripple Performance of the Proposed Control

The CR and power losses of the converter as functions of both m_a and the number of inserted SMs are plotted in Fig. 7.9. With the insertion/bypass of SMs, the converter can achieve an even larger output voltage range than the one achieved by only modulating the m_a index. As shown in Fig. 7.9, the power losses of the converter are actually maintained during the PDT-based control or even reduced with an m_a in the range of 0.4 to 0.8. The reason is that during the PDT, the gate pulses are dropped, resulting in a much smaller



(a)

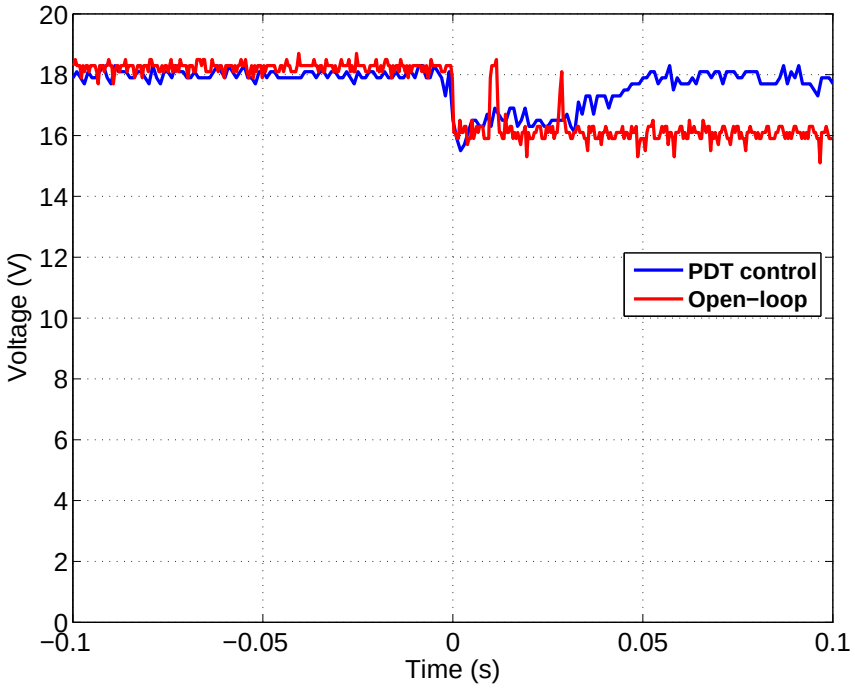


(b)

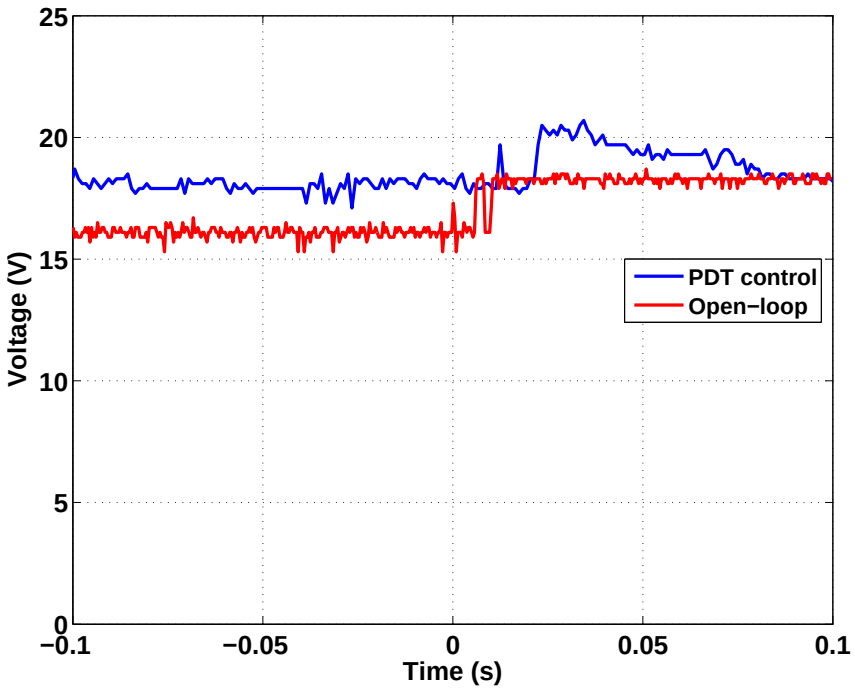
Figure 7.6: Output voltage (channel 1) and the PDT gate signal (channel 2) of the MMC3 with an output voltage reference of 18.8 V and input voltage of (a) 4.42 V and (b) 5.02 V.

gate drive loss. The RMS current in the system is also reduced even with an increased peak amplitude due to a shorter on-time of the switches, as shown in Fig. 7.10 where an $m_a = 0.2$ is used. However, it is still desirable to bypass a SM to avoid the high power losses at very low m_a index below 0.2.

The output voltage ripple performance under open-loop and closed-loop operation is also compared in Fig. 7.11. In Fig. 7.11(a), the peak-to-peak output voltage ripple is almost 2 V. Even neglecting the high-voltage spikes during the switching transients, the voltage ripple read from Fig. 7.11(a) is about 0.3 V, which is still much higher compared with the estimated one in Table 5.3. The main reason leading to this difference is that the output capacitor has an ESR of about 80 mΩ. Considering a peak charging current of more than 5 A, this resistance will generate significant amount of voltage ripple. The voltage ripple performance will become even worse when the PDT is in use as in Fig. 7.11(b). To solve this problem, multiple output capacitors must be connected in parallel to reduce the effect of capacitor ESR.

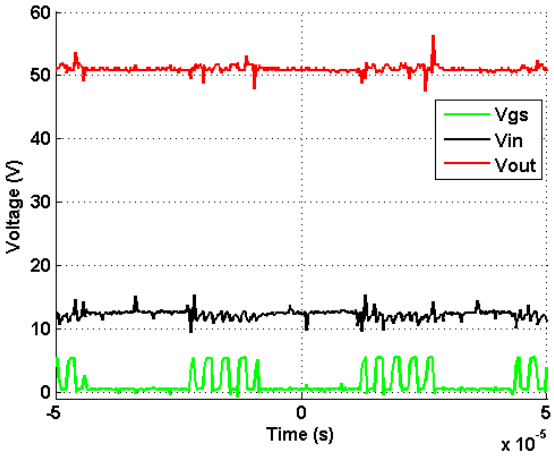


(a)

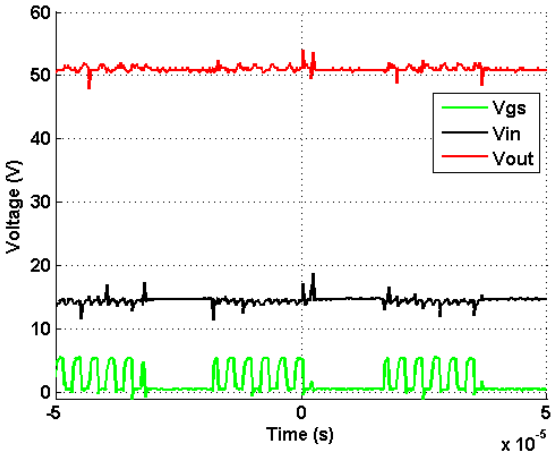


(b)

Figure 7.7: The output voltage of the MMC3 under the PDT feedback and open-loop control strategies when subjected to a load resistance change from (a) 100 Ω to 50 Ω and (b) 50 Ω to 100 Ω.



(a)



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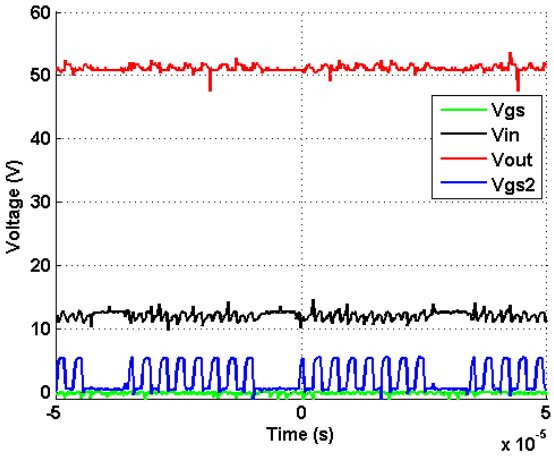


(c)

Figure 7.8: Output voltage, input voltage and gate signals of the converter with (a) 50 Ω and (b) 33 Ω load and (c) increased input voltage.

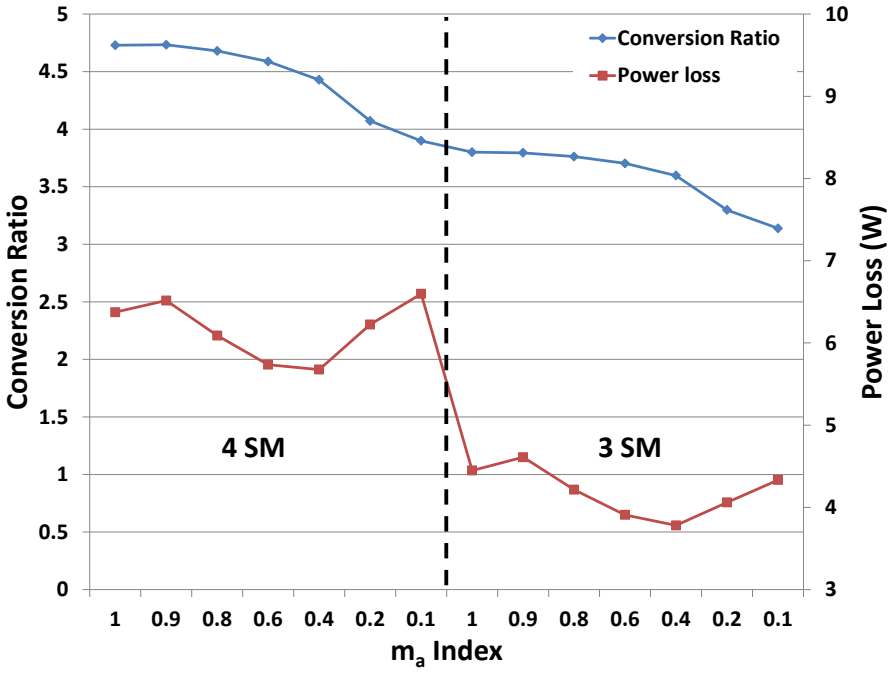
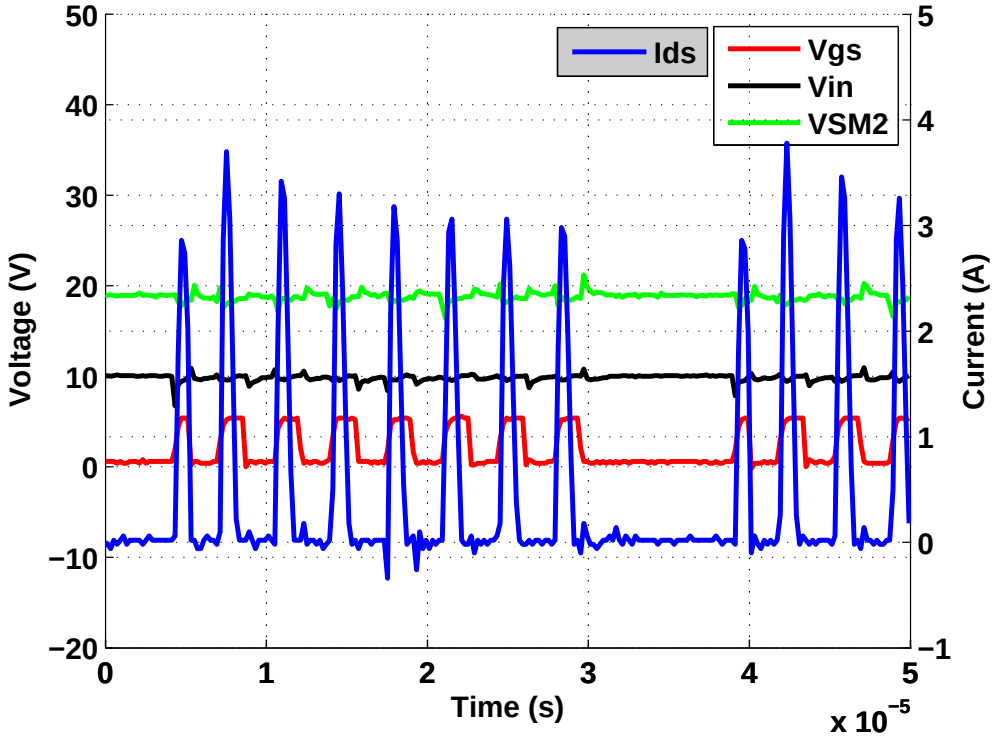
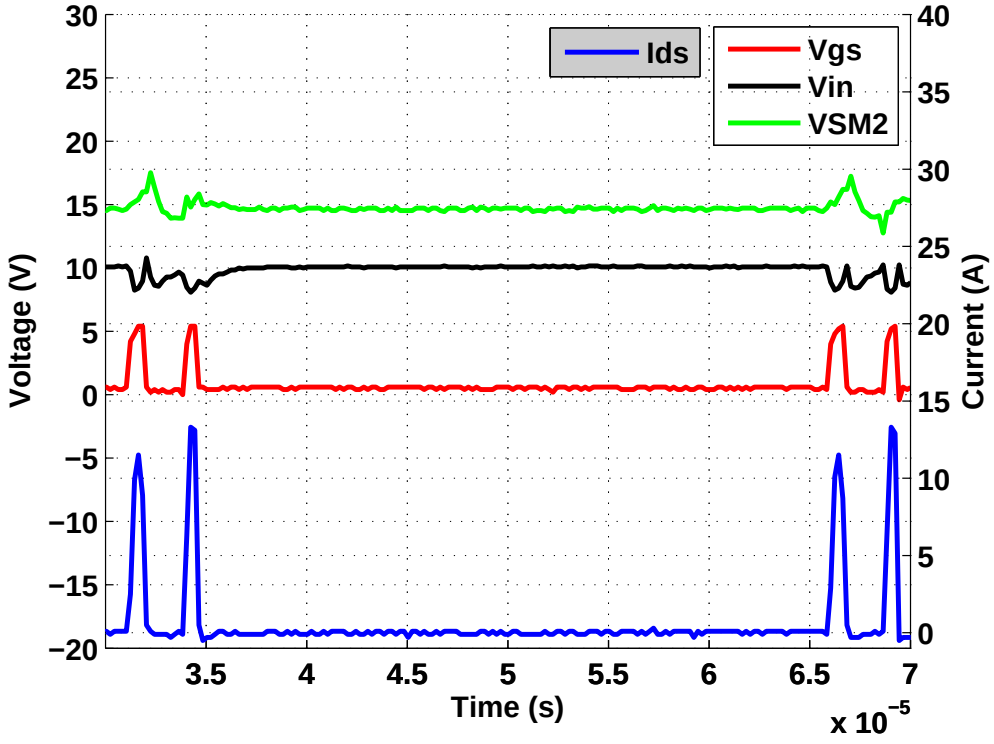


Figure 7.9: The CR and power losses of the converter with 3 or 4 SMs for different m_a indices.

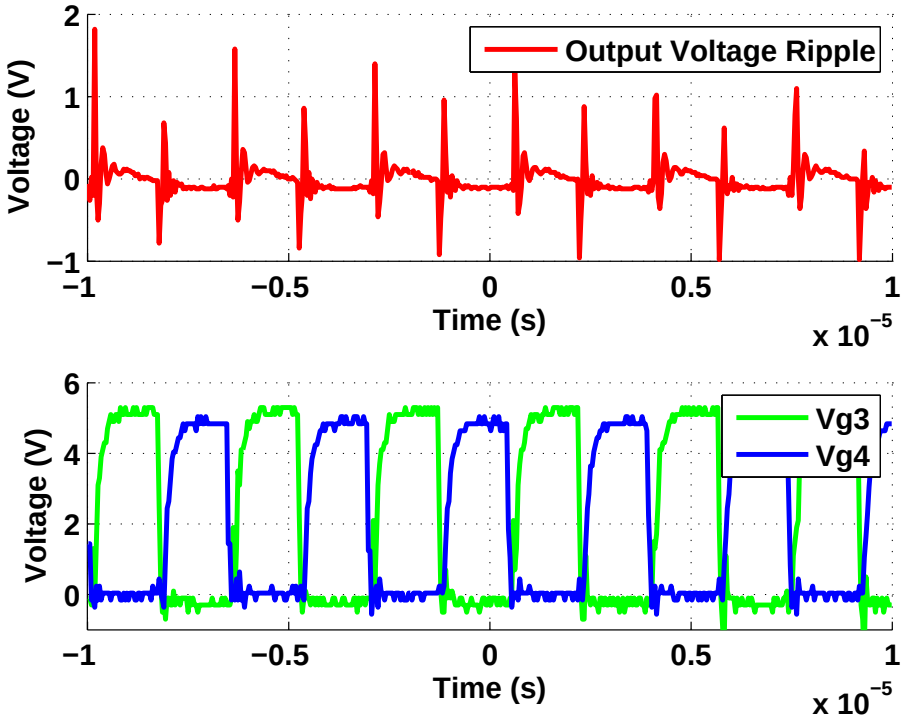


(a)

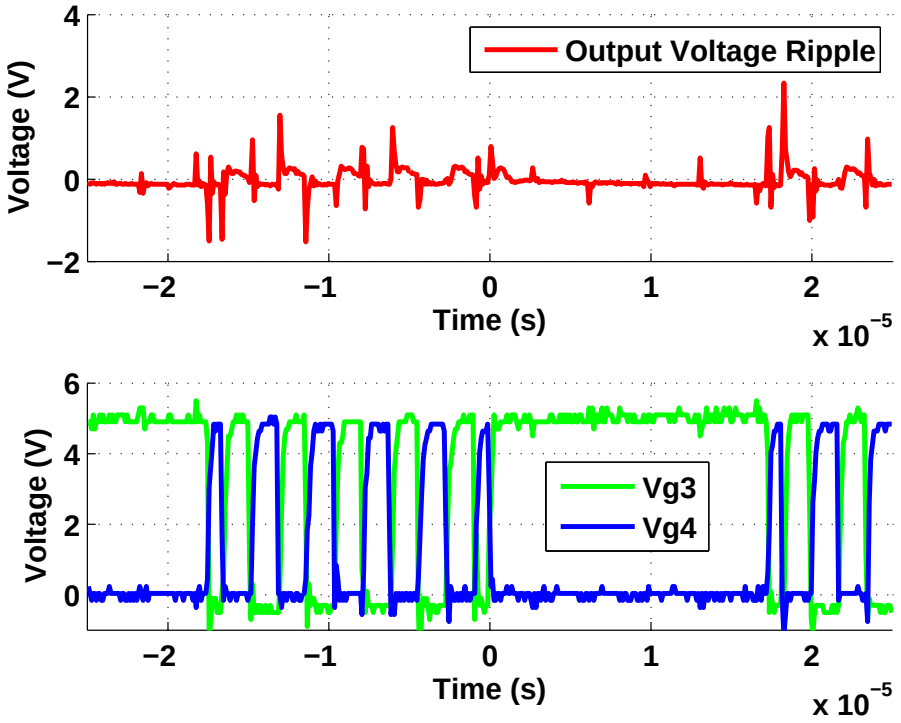


(b)

Figure 7.10: Switching current waveforms of SM2 during operations with (a) m_a=0.6 and (b) m_a=0.2.



(a)



(b)

Figure 7.11: Output voltage ripple during operations with (a) open-loop control and (b) m_a=0.5.

CHAPTER 8
CONCLUSIONS AND FUTURE RESEARCH

8.1 Contributions

The main contributions of this thesis are:

- A closed-loop output voltage control method is proposed for the Modular Multilevel Clamped Capacitor Converter (MMC3) based on a combination of the Pulse Dropping Technique (PDT) and insertion/bypass of SubModules (SMs). The closed-loop MMC3 can output an arbitrary voltage and reject both source- and load-side disturbances and maintain a desired voltage level.

- A detailed time-domain model is developed for the MMC3 to accurately calculate the output and SM capacitor voltages as well as the capacitor current. The effect of parasitic inductance is analyzed and the possibility and requirement to achieve Zero Current Switching (ZCS) are discussed. The effects of PDT and insertion/bypass of SMs are also taken into account.

- A state-space small-signal model is developed for the MMC3 to evaluate the stability of the proposed control strategy.

- A Dickson converter prototype is designed and built to experimentally validate the proposed control strategy. The prototype is tested up to 170 W with a peak efficiency of 93.8% and a detailed power loss analysis is carried out. The capability of the proposed closed-loop control strategy to reject both source- and load-side disturbances is also validated. Power loss and output ripple performance of the closed-loop system are also discussed.

- A multi-objective optimal design problem is formed to select power devices and main design parameters of a Dickson converter based on given system specifications and operation constraints. Peak efficiency of 96.5% can be expected if better power devices are used, deadtime is shortened and a more efficient way to protect devices from cross-talk issues is applied.

- An electro-thermal model for GaN FETs is developed in LTSPICE environment. The model represents the mutual effects between electrical characteristics and junction temperature to give accurate estimations of junction temperature in circuit simulations. The model is validated through both simulation and experimental tests.

8.2 Future Research

- Improvements need to be carried out on the Dickson converter prototype based on the optimal design to further increase its efficiency and gain more insights into its design for high performance.

- The souce of large voltage spikes in the output voltage needs to be identified and suppressed for a cleaner system output.

- A circuit to protect power devices from cross-talk issues with a lower power loss is needed to fully utilize the advantages of GaN power devices in the Dickson converter.

- A thorough comparison of the proposed control strategy with other possible control strategies is needed to identify the tradeoffs of using the propose method.

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